TRENTON Systems, Inc.
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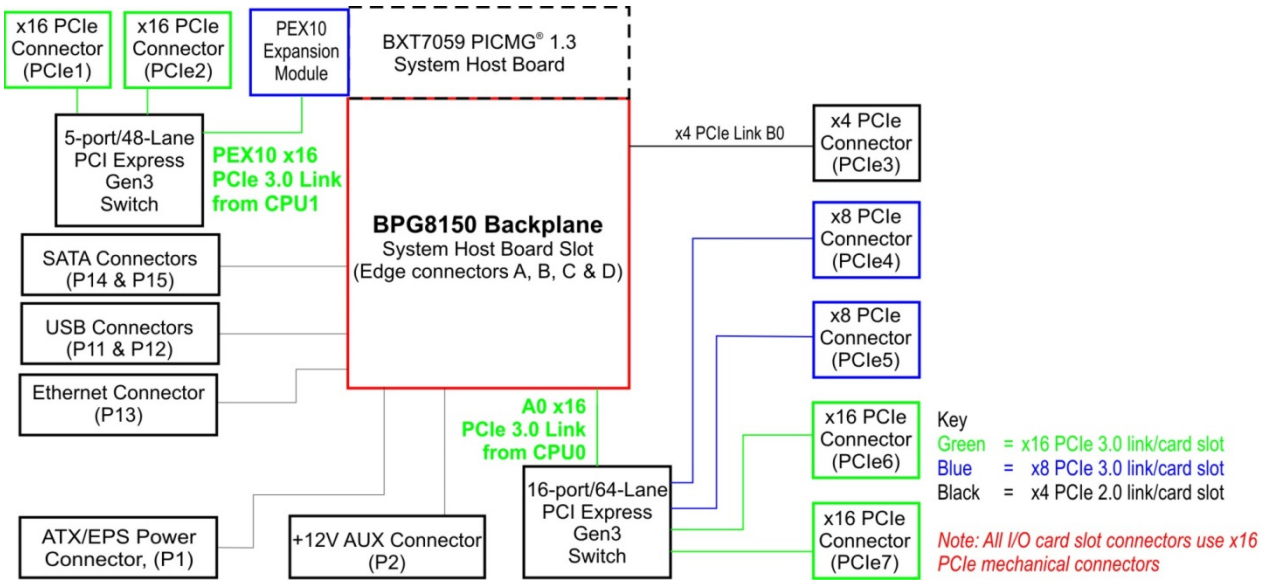
# Technical Information –Jumpers, Connectors and Status LEDs
# BPG8150 (8150) Small Form Factor PCI Express 3.0 Backplane

## Block Diagram




**BPG8150 Block Diagram Key**
**Green = x16 PCIe Gen3 links**
**Blue = x8 PCIe Gen3 links**
**Black = x4 PCIe Gen2 link**
*Note: All I/O card slot connectors use x16 PCIe mechanical connectors*

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**NOTE:** The BPG8150 backplane is optimized for use with dual-processor PCI Express 3.0 system host boards such as the Trenton BXT7059. Non-Gen3 dual-processor PICMG 1.3 SHBs; such as the JXT6966 may be used with the BPG8150 backplane, but the PCIe root links to the Gen3 switches will be operating at PCIe 2.0 link speeds. For the JXT6966 usage case, all downstream links from the Gen3 switches will deliver PCIe 3.0 link speeds when a Gen3 PCIe card (i.e. endpoint) is installed in PCI Express option card slots PCIe1, PCIe2, and PCIe4 through PCIe7. In either SHB usage case a PEX10 option card must be used with the BXT7059 or JXT6966 to provide the interface from the boards' CPU1 to the 5-port/48-lane PCIe Gen3 switch.

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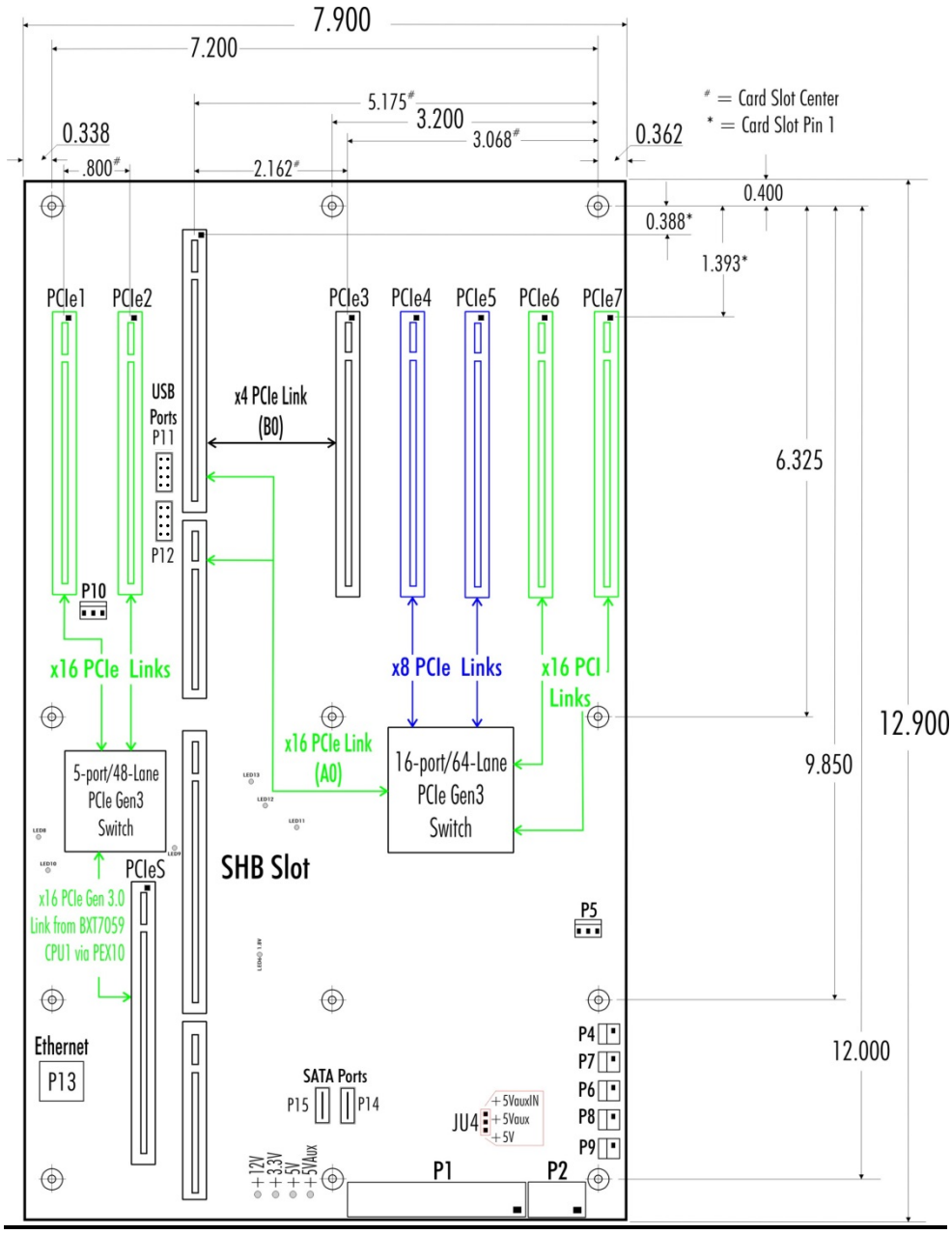
## Layout Diagram – 8150-009 – Dimension Drawing




**Notes:**

1. Connector spacing: 0.800”
2. Power connectors shown represents backplane model number 8150-009
3. The nominal backplane thickness is 0.080”; however, the backplane mounting holes are recessed 0.018” on the bottom to provide an effective PCB thickness of 0.062” for use in the chassis design process.
4. Mounting holes: .156” diameter
5. All dimensions are in inches.
6. Optional PICMG 1.3 USB, SATA and Ethernet connectivity provided by Trenton PICMG 1.3 SHBs. Not all SHBs support these capabilities.
7. Refer to the status LED section for definitions on the PCI Express link speed and state for each diagnostic LED

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## 8150-009 Configuration Jumpers

The setup of the configuration jumpers on the backplane is described below. An * indicates the jumper default value.

**NOTE:** For the JU4 3-pin / two-position jumper, "TOP" refers to positioning of the two jumper pins that are closest to the I/O card slots.

| Jumper | Description |
|---|---|
| **JU4** | **+5V Auxiliary Voltage** (3-pin Jumper/Two Position)<br>Install on the TOP (pins 2-3) if the +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies. *<br><br>Install on the BOTTOM (pins 1-2) if the +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non- ATX/EPS power supplies. |

***Default position**

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## 8150-009 Connectors

**NOTE:** Pin 1 on the connectors is indicated by the square pad on the PCB.

**P1 - ATX/EPS Power Connector**

24 pin right-angle dual row, Molex #39-30-1240

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +3.3V | 13 | +3.3V |
| 2 | +3.3V | 14 | NC |
| 3 | Gnd | 15 | Gnd |
| 4 | +5V | 16 | PSON# |
| 5 | Gnd | 17 | Gnd |
| 6 | +5V | 18 | Gnd |
| 7 | Gnd | 19 | Gnd |
| 8 | PWRGD | 20 | NC |
| 9 | +5VAUX | 21 | +5V |
| 10 | +12V | 22 | +5V |
| 11 | +12V | 23 | +5V |
| 12 | +3.3V | 24 | Gnd |

**P2 - +12V AUX Power Connector**

8 pin right-angle dual row, Molex #39-30-0080

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Gnd | 8 | +12V |
| 2 | Gnd | 7 | +12V |
| 3 | Gnd | 6 | +12V |
| 4 | Gnd | 5 | +12V |

**P4 - SMBUS Connector**

2 pin vertical single row header, Amp #640456-2

| Pin | Signal |
|---|---|
| 1 | SMDAT |
| 2 | SMCLK |

**P6 - Power-On Connector**

2 pin vertical single row header, Amp #640456-2

| Pin | Signal |
|---|---|
| 1 | PSON# |
| 2 | Gnd |

**P7 - Power Button Connector**

2 pin vertical single row header, Amp #640456-2

| Pin | Signal |
|---|---|
| 1 | PWRBT# |
| 2 | Gnd |

**P8 - Reset Connector**

2 pin vertical single row header, Amp #640456-2

| Pin | Signal |
|---|---|
| 1 | SHB_RST# |
| 2 | Gnd |

## 8150-009 Connectors (continued)

**P9 - Power Good Connector**
2 pin vertical single row header, Amp #640456-2

| Pin | Signal |
|---|---|
| 1 | PWRGD |
| 2 | +5V |

**P11 - Universal Serial Bus (USB) Connector**[#]
8 pin dual row header, Amp #5103308-1

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V-USB1 | 2 | +5V-USB0 |
| 3 | USB1- | 4 | USB0- |
| 5 | USB1+ | 6 | USB0+ |
| 7 | Gnd-USB1 | 8 | Gnd-USB0 |

**P12 - Universal Serial Bus (USB) Connector**[#]
8 pin dual row header, Amp #5103308-1

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V-USB3 | 2 | +5V-USB2 |
| 3 | USB3- | 4 | USB2- |
| 5 | USB3+ | 6 | USB2+ |
| 7 | Gnd-USB3 | 8 | Gnd-USB2 |

**P13 - 10/100/1000Base-T Ethernet Connector – LAN 0**[#]
8 pin vertical RJ-45 connector, Molex #42878-8410

| Pin | Signal |
|---|---|
| 1 | TRP1+ |
| 2 | TRP1- |
| 3 | TRP2+ |
| 4 | TRP3+ |
| 5 | TRP3- |
| 6 | TRP2- |
| 7 | TRP4+ |
| 8 | TRP4- |

**P14, P15 SATA Connectors (2)**[#]
7 pin vertical connector with latch, Molex # 67800-8005

| Pin | Signal |
|---|---|
| 1 | Gnd |
| 2 | TX0_p |
| 3 | TX0_n |
| 4 | Gnd |
| 5 | RX0_p |
| 6 | RX0_n |
| 7 | Gnd |

[#]Backplane functionality provided by the system host board

## 8150-009 Diagnostic LED Status – Power Indicators

| LED Reference Designation | Backplane Silkscreen Wording | LED On | LED Off |
|---|---|---|---|
| LED1 | +5AUX | Voltage Detected | Voltage Not Detected |
| LED2 | +5V | Voltage Detected | Voltage Not Detected |
| LED3 | +3.3V | Voltage Detected | Voltage Not Detected |
| LED4 | +12V | Voltage Detected | Voltage Not Detected |
| LED6 | PWRGD 1.8V | Voltage Detected | Voltage Not Detected |

## 8150-009 Diagnostic LED Functions – PCI Express Links

| LED Reference Designation | Backplane Silkscreen Wording | Function |
|---|---|---|
| LED8 | EEPROM PROG | Programming error for the EEPROM values used by PCIe Switch U30 (12-port/48-lane PCIe Gen3 switch) |
| LED9 | EEPROM | U30 EEPROM status LED |
| LED10 | PEX10 LINKGD | Indicates PCIe link status between PCIe Switch U30 and CPU1 on the SHB connected via the SHBs PEX10 option card |
| LED11 | EEPROM PROG | Programming error for the EEPROM values used by PCIe Switch U50 (16-port/64-lane PCIe Gen3 switch) |
| LED12 | EEPROM | U50 EEPROM status LED |
| LED13 | LINKA0GD | Indicates A0 link established between CPU0 on the SHB and PCIe Switch U50 (16-port/64-lane PCIe Gen3 switch) |

## 8150-009 Diagnostic LED10 and LED13 – PCI Express Link Status for the PCIe Switches

| LED Pattern | PCI Express Link State |
|---|---|
| OFF | Link down |
| ON | Link is up and running at PCIe Gen3 speed (8.0GT/s) |
| Blinking, 0.25 sec. ON, 0.25 sec. OFF | Link is up and running at PCIe Gen2 speed (5.0GT/s) |
| Blinking, 0.5 sec. ON, 0.5 sec. OFF | Link is up and running at PCIe Gen1.1 speed (2.5GT/s) |