SLE

5891-xxx

No. 87-005894-000 Revision G

TECHNICAL REFERENCE

Pentium® III

PROCESSOR-BASED

SBC

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Return company address and contact
Model name and model # from the label on the back of the board
Serial number from the label on the back of the board
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Utica, NY facility:

TRENTON Technology Inc.
1001 Broad Street
Utica, NY 13501
Attn: Repair Department

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HANDLING PRECAUTIONS

WARNING: This product has components which may be damaged by electrostatic discharge.

To protect your single board computer (SBC) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SBC in its static-shielded bag until you are ready to perform your installation.
- Handle the SBC by its edges.
- Do not touch the I/O connector pins. Do not apply pressure or attach labels to the SBC.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

SOLDER-SIDE COMPONENTS

This SBC has components on both sides of the PCB. It is important for you to observe the following precautions when handling or storing the board to prevent solder-side components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

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Chapter 1 Specifications

INTRODUCTION

The SLE full-featured PCI/ISA processors are single board computers (SBCs) which feature dual Intel® Pentium® III (FC-PGA) microprocessors, ServerWorks ServerSet™ III LE chipset, 133MHz system and memory buses, Intel 69030 video interface, 2GB SDRAM, PCI Local Bus, cache, floppy controller, dual EIDE (Ultra DMA/33) interfaces, PCI Ultra3 SCSI controller, dual PCI 10/100Base-T Ethernet controllers, two serial ports, parallel port, speaker port and mouse/keyboard port on a single ISA-size card. These single-slot, high performance SBCs plug into PICMG® PCI/ISA passive backplanes and provide full PC compatibility for the system expansion slots.

MODELS

Model #	Model Name	Speed
5891-603-xM	SLE/1.4	1.4GHz
5891-602-xM	SLE/1.26	1.26GHz
5891-601-xM	SLE/1.13	1.13GHz
5891-407-xM	SLE/1.0B	1.0GHz
5891-406-xM	SLE/933	933GHz
5891-405-xM	SLE/866	866GHz
5891-404-xM	SLE/800EB	800GHz
5891-403-xM	SLE/733	733GHz
5891-402-xM	SLE/667	667GHz
5891-401-xM	SLE/600EB	600MHz

where xM indicates memory size (0M = 0MB memory, 8M =8MB memory, etc.)

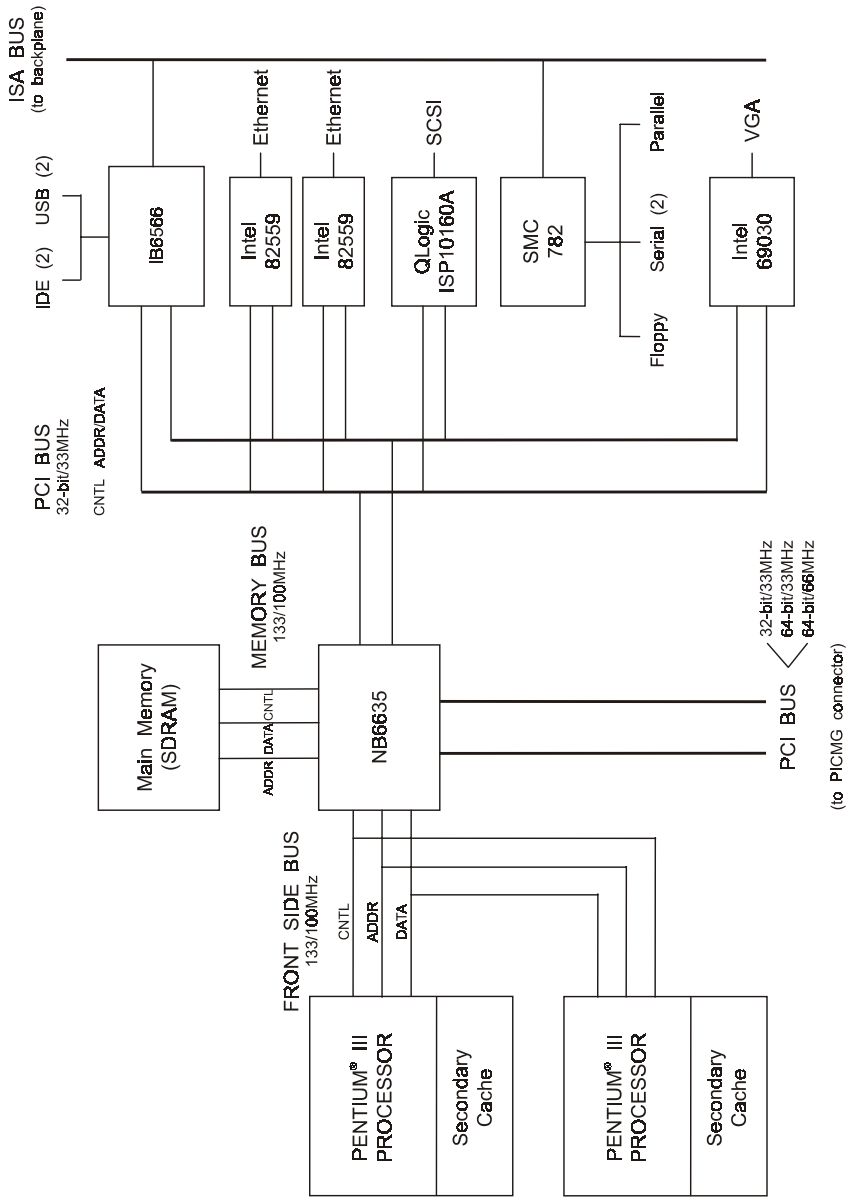
FEATURES

- Intel® Pentium® III (FC-PGA) microprocessors
  - 1.4GHz, 1.26GHz or 1.13GHz with 512K cache
  - 1.0BGHz, 933MHz, 866MHz, 800EBMHz, 733MHz, 667MHz or 600EBMHz with 256K cache
- ServerWorks ServerSet III LE chipset with 133MHz system and memory buses
- Dual microprocessors using Symmetric Multiprocessing (SMP)
- PCI Local Bus operating in 64-bit/66MHz, 64-bit/33MHz or 32-bit/33MHz mode
- Super VGA on-board video interface (Intel 69030)
- PCI Local Bus supports off-board PCI option cards, dual PCI 10/100Base-T Ethernet controllers and on-board PCI Ultra3 SCSI controller (QLogic ISP10160A)
- DRAM error checking and correction (ECC) support
- Compatible with PCI Industrial Computer Manufacturers Group (PICMG) 1.0 Specification

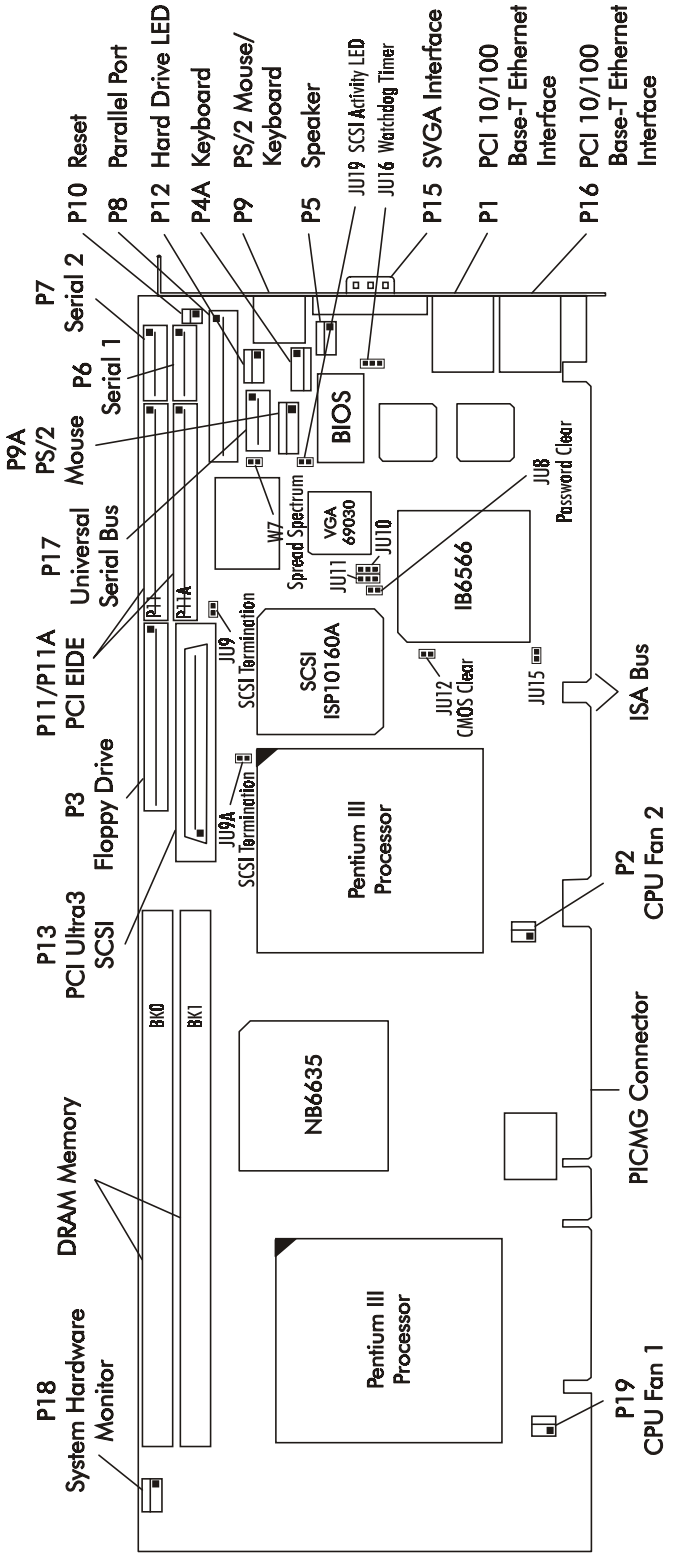
FEATURES (CONTINUED)

- Supports up to 2GB of Synchronous DRAM (SDRAM) on-board
- Floppy drive and dual PCI EIDE Ultra DMA/33 drive interfaces
- Two serial ports and one parallel port
- Automatic or manual peripheral configuration
- Watchdog timer
- System hardware monitor
- Shadow RAM for System BIOS and peripherals increases system speed and performance
- Full PC compatibility

SBC BLOCK DIAGRAM



SBC PROCESSOR BOARD LAYOUT



PROCESSORS

- Two Intel® Pentium® III microprocessors
  - 1.4GHz, 1.26GHz or 1.13GHz with 512K cache
  - 1.0BGHz, 933MHz, 866MHz, 800EBMHz, 733MHz, 667MHz or 600EBMHz with 256K cache
- Processors use the Socket 370 Flip Chip Pin Grid Array (FC-PGA) packaging

BUS INTERFACES ISA and PCI Local Bus compatible

DATA PATH DRAM/Memory - 64-bit

ISA Bus - 16-bit

PCI Bus - 32-bit or 64-bit

Video - 32-bit

BUS SPEED - ISA 8.33MHz

BUS SPEED - PCI 33MHz or 66MHz

BUS SPEED - SYSTEM & MEMORY 133MHz Front Side Bus

SYSTEM & MEMORY BUSES The ServerWorks ServerSet III LE chipset supports the system and memory buses at 133MHz, which provides a higher bandwidth path for transferring data between main memory/chipset and the processors.

DMA CHANNELS The SBC is fully PC compatible with seven DMA channels, each supporting type F transfers.

INTERRUPTS The SBC is fully PC compatible with interrupt steering for PCI plug and play compatibility.

BIOS (FLASH) The BIOS is an AMIBIOS with built-in advanced CMOS setup for system parameters, peripheral management for configuring on-board peripherals, PCI-to-PCI bridge support and PCI interrupt steering. The BIOS chip is a boot block Flash device - 28F002BX or 28F004BT. The BIOS may be upgraded from floppy disk by pressing **<Ctrl>** + **<Home>** *immediately* after reset or power-up with the floppy disk in drive A:. Custom BIOSs are available.

CACHE MEMORY The Pentium III processors include integrated on-die, 256K or 512K 8-way set associative level two (L2) cache. The L2 cache implements the Advanced Transfer Cache architecture with a 256-bit wide bus. The processors also include a 16K level one (L1) instruction cache and 16K L1 data cache. These cache arrays run at the full speed of the processor core.

DRAM MEMORY

The DRAM interface consists of two dual in-line memory module (DIMM) sockets and supports auto detection of memory up to 2GB of Synchronous DRAM (SDRAM). The System BIOS automatically detects memory type, size and speed.

The SBC uses industry standard 72-bit wide gold finger DIMM SDRAM modules in two 168-pin DIMM sockets.

NOTE: Memory can be installed in one or both DIMM sockets. If only one DIMM module is used, it must be populated in the top DIMM socket (Bank 0 - BK0). If two modules are used, they must be the same DIMM type, but may be different sizes (see table below). EDO DIMMs and unbuffered SDRAM DIMMs are not supported. All DIMMs must have gold contacts.

The SBC supports DIMM memory modules which are PC-133 compliant and have the following features:

- 168-pin DIMMs with gold-plated contacts
- 133MHz SDRAM
- ECC (72-bit) memory
- 3.3 volt
- Registered configuration

The following DIMM sizes are supported:

DIMM Size	DIMM Type	ECC
64MB	Registered	8M x 72
128MB	Registered	16M x 72
256MB	Registered	32M x 72
512MB	Registered	64M x 72
1GB	Registered	128M x 72

All memory components and DIMMs used with the SBC must be PC-133 compliant, which means that they comply with IBM's PC133 SDRAM Registered DIMM Design Specification.

ERROR CHECKING AND CORRECTION

The memory interface supports ECC modes via BIOS setting for multiple-bit error detection and correction of all errors confined to a single nibble.

PCI LOCAL BUS INTERFACE

The SBC is fully compliant with the PCI Local Bus 2.1 Specification. The SBC supports two independent PCI Bus interfaces: a 32-bit Primary PCI Bus interface (33MHz) and a 64-bit Secondary (33/66MHz) Bus interface. Both Primary and Secondary PCI Bus interfaces provide a sixteen deep I/O cache and a four deep request queue for PCI to memory cycles. Both the interfaces provide a four deep quad word write posting for PCI master cycles to memory. The I/O cache supports the MESI protocol of processor bus, thereby keeping the I/O cache data always coherent with the rest of the system.

The Primary PCI interface is 32 bits wide and runs at 33MHz. This bus supports the on-board SCSI, video and dual Ethernet interfaces.

The Secondary PCI interface is 64 bits wide and runs at 33/66MHz. This interface provides a sixteen-entry I/O cache and is routed off-board to drive PICMG compliant PCI/ISA passive backplanes.

The SBC supports PCI-to-PCI bridge technology, a pipelined snoop ahead feature and improved PCI to DRAM write-back policy. The PCI Local Bus interfaces to standard PCI option cards in the backplane and to the on-board PCI Ultra3 SCSI controller and dual PCI 10/100Base-T Ethernet controllers. The PCI Local Bus interface to the backplane is compliant with the PCI Industrial Computer Manufacturers Group (PICMG) 1.0 Specification.

UNIVERSAL SERIAL BUS (USB)

The SBC supports two USB 1.0 ports for serial transfers at 12 or 1.5Mbit/sec. The Universal Serial Bus (USB) is an interface allowing for connectivity to many standard PC peripherals via an external port.

SYMMETRIC MULTIPROCESSING (SMP)

The dual Pentium III processor-based design allows the operating system to assign tasks on demand to the next available processor. SMP uses applications which are divided into threads which can run concurrently on any available processor. This improves performance of the application itself as well as the total throughput of the system.

SUPER VGA INTERFACE

The Intel 69030 HiQVideo video interface integrates 4MB of high-speed SDRAM frame buffer memory into the chip.

By embedding SDRAM and graphics controller logic on the same die, the 69030 delivers uncompromising performance. The increase in the frame buffer bandwidth enables the 69030 to support high-color, high-resolution graphics modes and real-time video acceleration. The interface supports pixel resolutions up to 1280 x 1024 x True Color non-interlaced. Software drivers for enhanced performance and resolution are available for most popular operating systems.

SYSTEM HARDWARE MONITOR

The system hardware monitoring system monitors system voltages, temperature and fan speeds.

The circuitry is based on National Semiconductor's LM80. The LM80 monitors seven system voltages, two fan speeds and the board ambient temperature. All of the voltages, fan speeds and temperature measurements have associated programmable watchdog limits. When any of these programmed limits are exceeded, the monitor software can be used to notify the SBC. In addition, the externally available OS# signal can be used to notify external hardware of any over-temperature condition.

Fan speed monitoring can be configured to monitor two system fans.

The LM80 also monitors an external chassis intrusion switch via the system hardware monitor connector (P18).

A general purpose output (GPO) is also provided at the system hardware monitor connector. This signal can be used to provide a user-defined function.

The following system voltages are monitored by the LM80:

- -12 volts
- 3.3 volts provided by the on-board voltage regulator for components on the SBC
- 3.3 volts backplane power used by the option slots
- +5 volts
- +12 volts
- VCC_CORE, voltage provided by on-board VRM
- 1.5 volt, VTT voltage used by processor's GTL+ bus

PCI 10/100BaseT Ethernet Interfaces (Dual)

The dual PCI Ethernet interfaces are implemented using two Intel 82559 Ethernet controllers and operate in 10Base-T and 100Base-TX Fast Ethernet modes. The interfaces are compliant with IEEE 802.3 and PCI Local Bus 2.1 Specifications.

The main components of each interface are:

- Intel 82559 for 10/100-Mb/s media access control (MAC) with SYM, a serial ROM port and a PCI Bus Master interface
- Serial ROM for storing the Ethernet address and the interface configuration and control data
- Integrated RJ-45/Magnetics module connector on the SBC's I/O bracket for direct connection to the network. The connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection.
- Link status and activity LEDs on the I/O bracket for status indication (See *Ethernet LEDs and Connectors* later in this chapter.)

Software drivers are supplied for most popular operating systems.

PCI SCSI Interface

The SCSI interface supports Ultra3 SCSI data transfer using QLogic's ISP10160A SCSI controller, which supports SCSI data transfer up to 160MB per second. The interface is Ultra3 LVD, which may be used with high performance drives, such as Ultra 160 drives, to get maximum performance. The Ultra3 features of this channel are double-edge clocking, domain validation and cyclical redundancy checking.

Active termination is provided with terminator voltage protected by self-resetting fuses. Two jumpers (JU9 and JU9A) are provided to disable the termination (see the *Configuration Jumpers* section later in this chapter). Software drivers are available for most popular operating systems.

The QLogic Fast!UTIL Configuration Utility allows you to view and/or change the default configuration settings for the Ultra3 SCSI adapter. You may press **<Alt>** + **<Q>** to invoke the configuration utility.

PCI ENHANCED IDE INTERFACES (DUAL)

Dual high performance PCI Bus Master EIDE interfaces are capable of supporting two IDE disk drives each in a master/slave configuration. The interfaces support Ultra DMA/33 with synchronous DMA mode transfers up to 33MB per second.

FLOPPY DRIVE INTERFACE

The SBC supports two floppy disk drives. Drives can be 360K to 2.88MB, in any combination.

SERIAL INTERFACE

Two high-speed FIFO (16C550) serial ports with independently programmable baud rates are supported. The IRQ for each serial port has BIOS selectable addressing.

ENHANCED PARALLEL INTERFACE

The SBC provides a PC/AT compatible bidirectional parallel port and supports enhanced parallel port (EPP) mode and extended capabilities port (ECP) mode. The ECP mode is IEEE 1284 compliant. The IRQ for the parallel port has BIOS selectable addressing.

PS/2 MOUSE INTERFACE

The SBC is compatible with a PS/2-type mouse. The mouse connection can be made by using either the PS/2 mouse header or the bracket mounted mouse/keyboard mini DIN connector. The mouse may be connected directly to the mini DIN connector or to the "mouse" side of the "Y" adapter. Mouse voltage is protected by a self-resetting fuse.

KEYBOARD INTERFACE

The SBC is compatible with an AT-type keyboard. The keyboard connection can be made by using either the keyboard header or the "keyboard" side of the "Y" adapter plugged into the bracket mounted mouse/keyboard mini DIN connector. Keyboard voltage is protected by a self-resetting fuse.

WATCHDOG TIMER

The watchdog timer is a hardware timer which resets the SBC if the timer is not refreshed by software periodically. The timer is typically used to restart a system in which an application becomes hung on an external event. When the application is hung, it no longer refreshes the timer. The watchdog timer then times out and resets the SBC.

The watchdog timer has two levels of enable. First, the watchdog timer jumper must be moved to the "enabled" position, which puts the watchdog timer under software control.

The second level involves software control of the watchdog's timer retriggering. The SouthBridge (U8) General Purpose Port Register (GPM) at I/O address C52(h) must be set to a 0B(h), which blocks the triggering clock to the watchdog timer circuit, thus scheduling a hardware reset in about 1.5 seconds.

To refresh the watchdog timer, the software in the application must toggle bit 3 of the GPM register. First, a 0F(h) must be written to the GPM register to clear the watchdog timer delay; then the register must be set to a 0B(h), which schedules a system reset in 1.5 seconds. The toggling of bit 3 as specified must occur within a period of less than 1.5 seconds to insure that a system reset is not issued.

A set of watchdog timer software code and sample programs are available from Technical Support.

POWER FAIL DETECTION

A hardware reset is issued when on-board +5V voltage drops below 4.75 volts. In addition, if the 3.3V Monitor jumper (JU15) is enabled, a reset is issued if 3.3V is below tolerance. (See the *Configuration Jumpers* section later in this chapter.)

BATTERY

A built-in lithium battery is provided, for ten years of data retention for CMOS memory.

CAUTION: There is a danger of explosion if the battery is incorrectly replaced. Replace it only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

POWER REQUIREMENTS

+5V Typical

1.26GHz	14.95 Amps	
1.0GHz	14.02 Amps	Rev. L-07 and later
1.0GHz	13.6 Amps	Rev. K-06 and earlier
866MHz	11.4 Amps	
733MHz	10.5 Amps	
667MHz	7.8 Amps	

+12V @ 500 mAmps	Rev. L-07 and later
+12V @ 600 mAmps	Rev. K-06 and earlier

-12V @ < 100 mAmps

CAUTION: When configuring an SLE-based system with processor speeds of 1.0GHz or greater, the system integrator needs to ensure adequate power delivery. These high-speed processors can require the on-board voltage regulators (VRMs) to supply greater than 20 Amps to each processor. The input source voltage of the VRMs is the +5 volts that is sourced to the SBC through both the PCI and ISA card edge fingers. Even with VRM efficiency of 90%, this translates into a +5V current requirement in excess of 14 Amps.

With this high +5V current requirement, along with the 5-volt +/- 5% tolerance requirement, it is important that the power delivery system is adequate to provide a reliable +5 volts. An inadequate power delivery system will result in the +5V rail on the SLE SBC to drop below 4.75 volts under high current conditions, resulting in random system resets.

The single most important item in the power delivery system is the power supply. The integrator should choose a power supply that will minimize the DC voltage drop from the supply to the system backplane when delivering high currents. The gauge of the power supply's wires, number of wires and the type of connectors used are key items to consider. Most of today's high wattage (400W) power supplies will address all of these issues.

TEMPERATURE/ ENVIRONMENT

Operating Temperature:	0° C. to 50° C. for 1.26GHz and above 0° C. to 45° C. for 1.0GHz 0° C. to 50° C. for 933MHz 0° C. to 60° C. for 866MHz and below
Storage Temperature:	- 40° C. to 70° C.
Humidity:	5% to 90% non-condensing

MEAN TIME BETWEEN FAILURES (MTBF)

148,000 POH (Power-On Hours) at 40° C., per Bellcore

UL RECOGNITION

This SBC is a UL recognized product listed in file #E208896.

This board was investigated and determined to be in compliance under the Bi-National Standard for Information Technology Equipment. This included the Electrical Business Equipment, UL 1950, Third Edition, and CAN/CSA C22.22 No. 950-95.

CONFIGURATION JUMPERS

The setup of the configuration jumpers on the SBC is described below. * indicates the default value of each jumper.

NOTE: For two-position jumpers (3-post), "TOP" is toward the memory sockets; "BOTTOM" is toward the edge fingers.

Jumper	Description

JU8 **Password Clear**

Install for one power-up cycle to reset the password to the default (null password).
Remove for normal operation. *

JU9/JU9A **SCSI Termination - Channel 0**

These two jumpers may be used to enable or disable on-board active termination for the Ultra3 SCSI interface - Channel 0.

	JU9	JU9A
Enable active termination	Install *	Install *
Disable active termination	Remove	Remove
Enable upper byte only	Remove	Install

JU10/JU11 **System Flash ROM Operational Modes**

The Flash ROM has two programmable sections: the Boot Block for “flashing” in the BIOS and the Main Block for the executable BIOS and PnP parameters. Normally only the Main Block is updated when a new BIOS is flashed into the system.

	JU10	JU11
Program All (Boot and Main)	Top	Top
Normal PnP (Program Main Block)	Top *	Bottom *
Write Protect	Bottom	Bottom

JU12 **CMOS Clear**

Install to clear.
Remove to operate. *

NOTE: The CMOS Clear jumper works on power-up. To clear the CMOS, power down the system, install the jumper, then turn the power back on. CMOS is cleared during the POST routines. Wait for AMIBIOS to display a "CMOS Checksum Bad" message; then power down the system again and remove the jumper before the next power-up.

CONFIGURATION JUMPERS (CONTINUED)

Jumper	Description
JU15	**3.3V Monitor Enable** Install to enable the 3.3V monitor. Remove to disable the monitor. * **NOTE:** On SBCs with revision L-07 and later, the position of this jumper is horizontal; on earlier revisions it is vertical. **NOTE:** JU15 enables the 3.3 volt monitor, which monitors the 3.3V power plane of the backplane. This voltage is routed to the SBC via the PICMG connector. The monitor generates a RESET to the SBC if 3.3V is below tolerance. If your system does *not* supply 3.3V to the backplane, this jumper *must* be removed (disabled).
JU16	**Watchdog Timer** Install on the TOP to enable watchdog timer operation. Install on the BOTTOM for normal reset operation. *
JU19	**SCSI Activity LED Enable** Install to light the hard drive LED for SCSI drive activity. * Remove if you do not have a SCSI drive (i.e., the SCSI controller is not being used).
W7	**Spread Spectrum Enable** Install to enable spread spectrum for the processor oscillator, which may reduce EMI levels at some frequencies. * Remove to disable. **NOTE:** The W7 jumper is included on SBCs with revision J-05 and later. Revisions of H-04 and earlier do not have this jumper. On revisions L-07 and later, the default for W7 is "enabled"; on earlier revisions, the default was "disabled."

ETHERNET LEDS AND CONNECTORS

Each Ethernet interface has two LEDs for status indication and an RJ-45 network connector.

LED/Connector	Description
Link/Activity LED	Green LED which indicates the link status
Off	The Ethernet interface did not find a valid link on the network connection. Transmit and receive are not possible.
On (solid)	The Ethernet interface has a valid link on the network connection and is ready for normal operation. The Speed LED identifies connection speed.
On (flashing)	Indicates network transmit or receive activity.
Speed LED	Amber LED which identifies the connection speed.
Off	Indicates a 10Mb/s connection.
On	Indicates a 100Mb/s connection.
RJ-45 Network Connector	The RJ-45 network connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection.

SYSTEM BIOS SETUP UTILITY

The System BIOS is an AMIBIOS with a ROM-resident setup utility. The BIOS Setup Utility allows you to select the following categories of options:

- Main Menu
- Advanced Setup
- Chipset Setup
- PCIPnP Setup
- Boot Setup
- Security Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details are provided in the following chapters of this manual.

CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - PCI 10/100Base-T Ethernet Connector
8 pin shielded RJ-45 connector, Pulse #J0035D21B

Pin	Signal
1	TD+
2	TD-
3	RX+
4	NC
5	NC
6	RX-
7	NC
8	NC

P2 - CPU Fan 2
3 pin single row header, Molex #22-23-2031

Pin	Signal
1	Gnd
2	+12V
3	FanTach

P3 - Floppy Drive Connector
34 pin dual row header, Amp #103308-7

Pin	Signal	Pin	Signal
1	Gnd	2	N-RPM
3	Gnd	4	NC
5	Gnd	6	D-Rate0
7	Gnd	8	P-Index
9	Gnd	10	N-Motoron 1
11	Gnd	12	N-Drive Sel2
13	Gnd	14	N-Drive Sel1
15	Gnd	16	N-Motoron 2
17	Gnd	18	N-Dir
19	Gnd	20	N-Stop Step
21	Gnd	22	N-Write Data
23	Gnd	24	N-Write Gate
25	Gnd	26	P-Track 0
27	Gnd	28	P-Write Protect
29	Gnd	30	N-Read Data
31	Gnd	32	N-Side Select
33	Gnd	34	Disk Chng

CONNECTORS (CONTINUED)

P4A - Keyboard Header
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	Key
4	Kbd Gnd
5	Kbd Power (+5V fused) with self-resetting fuse

P5 - Speaker Port Connector
4 pin single row header, Amp #640456-4

Pin	Signal
1	Speaker Data
2	Key
3	Gnd
4	+5V

P6 - Serial Port 1 Connector
10 pin dual row header, Amp #103308-1

Pin	Signal	Pin	Signal
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send-I
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Signal Gnd	10	NC

P7 - Serial Port 2 Connector
10 pin dual row header, Amp #103308-1

Pin	Signal	Pin	Signal
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send-I
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Signal Gnd	10	NC

P8 - Parallel Port Connector
26 pin dual row header, Amp #103308-6

Pin	Signal	Pin	Signal
1	Strobe	2	Auto Feed XT
3	Data Bit 0	4	Error
5	Data Bit 1	6	Init
7	Data Bit 2	8	Slct In
9	Data Bit 3	10	Gnd

CONNECTORS (CONTINUED)

P8 - Parallel Port Connector (continued)

Pin	Signal	Pin	Signal
11	Data Bit 4	12	Gnd
13	Data Bit 5	14	Gnd
15	Data Bit 6	16	Gnd
17	Data Bit 7	18	Gnd
19	ACK	20	Gnd
21	Busy	22	Gnd
23	Paper End	24	Gnd
25	Slct	26	NC

P9 - PS/2 Mouse and Keyboard Connector
6 pin mini DIN, Kycon #KMDG-6S-BS-PS

Pin	Signal
1	Ms Data
2	Kbd Data
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Kbd Clock

P9A - PS/2 Mouse Header
6 pin single row header, Amp #640456-6

Pin	Signal
1	Ms Data
2	Reserved
3	Kbd Gnd
4	Kbd Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

P10 - External Reset Connector
2 pin single row header, Amp #640456-2

Pin	Signal
1	External Reset In (Low Active)
2	Gnd

P11 - Primary IDE Hard Drive Connector
40 pin dual row header, 3M #30340-6002HB

Pin	Signal	Pin	Signal
1	Reset	2	Gnd
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11

CONNECTORS (CONTINUED)

P11 - Primary IDE Hard Drive Connector (continued)

Pin	Signal	Pin	Signal
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 0	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	SELPDP
29	DACK 0	30	Gnd
31	IRQ 14	32	NC
33	Add 1	34	Gnd
35	Add 0	36	Add 2
37	CS 1P	38	CS 3P
39	IDEACTP	40	Gnd

P11A - Secondary IDE Hard Drive Connector
40 pin dual row header, 3M #30340-6002HB

Pin	Signal	Pin	Signal
1	Reset	2	Gnd
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 1	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	SELPDS
29	DACK 1	30	Gnd
31	IRQ 15	32	NC
33	Add 1	34	Gnd
35	Add 0	36	Add 2
37	CS 1S	38	CS 3S
39	IDEACTS	40	Gnd

CONNECTORS (CONTINUED)

P12 - Hard Drive LED Connector
4 pin single row header, Amp #640456-4

(This connector is used for both IDE and SCSI drives. See JU19 in the *Configuration Jumpers* section.)

Pin	Signal
1	+5V Pull-up
2	Light
3	Light
4	+5V Pull-up

P13 - PCI Ultra3 SCSI Controller Connector - Channel 0
50/68 pin high density connector, Amp #749069-7

Pin	Signal	Pin	Signal
1	SCD12	35	SCD#12
2	SCD13	36	SCD#13
3	SCD14	37	SCD#14
4	SCD15	38	SCD#15
5	SCDPH	39	SCDPH#
6	SCD0	40	SCD#0
7	SCD1	41	SCD#1
8	SCD2	42	SCD#2
9	SCD3	43	SCD#3
10	SCD4	44	SCD#4
11	SCD5	45	SCD#5
12	SCD6	46	SCD#6
13	SCD7	47	SCD#7
14	SCDPL	48	SCDPL#
15	Gnd	49	Gnd
16	DIFSENSE	50	Gnd
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	NC	53	NC
20	Gnd	54	Gnd
21	SCATN	55	SCATN#
22	Gnd	56	Gnd
23	SCBSY	57	SCBSY#
24	SCACK	58	SCACK#
25	SCRST	59	SCRST#
26	SCMSG	60	SCMSG#
27	SCSEL	61	SCSEL#
28	SCCD	62	SCCD#
29	SCREQ	63	SCREQ#
30	SCIO	64	SCIO#
31	SCD8	65	SCD#8
32	SCD9	66	SCD#9
33	SCD10	67	SCD#10
34	SCD11	68	SCD#11

CONNECTORS (CONTINUED)

P15 - PCI SVGA Interface Connector
15 pin VGA Ultra Compact connector, Kycon #K31-E15S-N

Pin	Signal	Pin	Signal	Pin	Signal
		6	Gnd		
1	Red			11	NC
		7	Gnd		
2	Green			12	EEDI
		8	Gnd		
3	Blue			13	HSYNC
		9	+5V		
4	NC			14	VSYNC
		10	Gnd		
5	Gnd			15	EECS

P16 - PCI 10/100Base-T Ethernet Connector
8 pin shielded RJ-45 connector, Pulse #J0035D21B

Pin	Signal
1	TD+
2	TD-
3	RX+
4	NC
5	NC
6	RX-
7	NC
8	NC

P17 - Universal Serial Bus (USB) Connector
8 pin dual row header, Molex #702-46-0821
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P18 - System Hardware Monitor Connector
4 pin single row header, Amp #640456-4

Pin	Signal
1	Gnd
2	GPO (General Purpose Output)
3	CI (Chassis Intrusion Input)
4	OS# (Temperature Sense Output)

CONNECTORS (CONTINUED)

P19 - CPU Fan 1

3 pin single row header, Molex #22-23-2031

Pin	Signal
1	Gnd
2	+12V
3	FanTach

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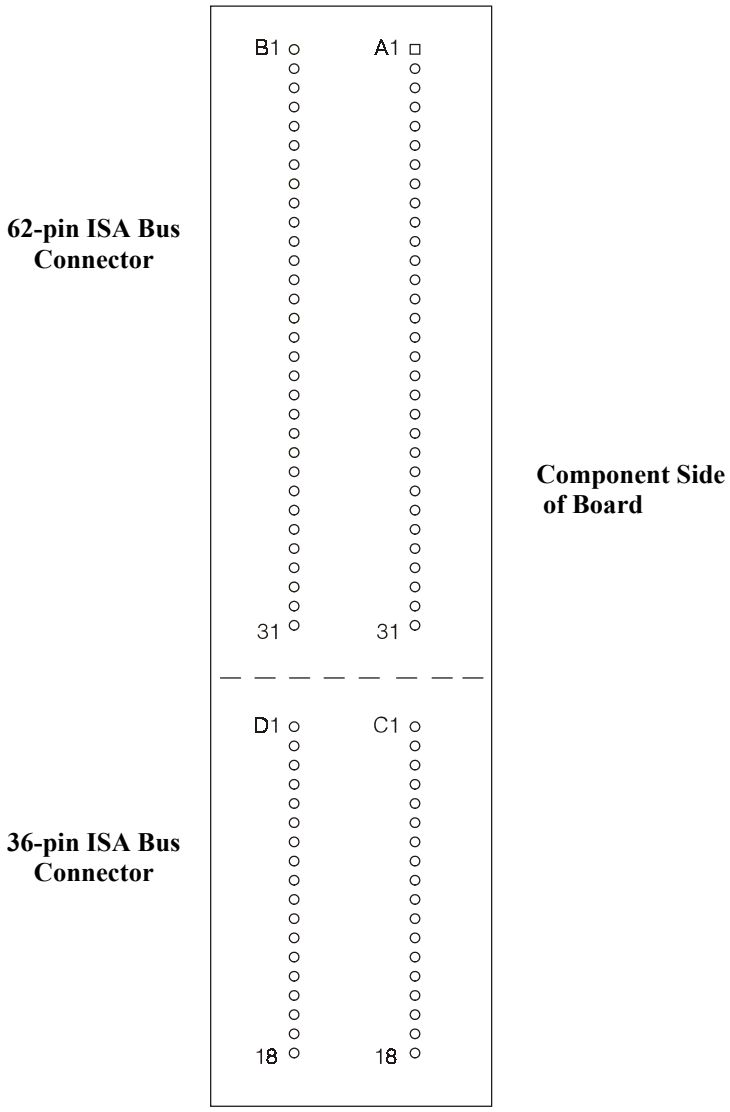
Chapter 2 ISA/PCI Reference

ISA BUS PIN NUMBERING



ISA BUS PIN ASSIGNMENTS

The following tables summarize pin assignments for the Industry Standard Architecture (ISA) Bus connectors.

I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
A1	IOCHK#	I	B1	Gnd	Ground
A2	D7	I/O	B2	RESDRV	O
A3	D6	I/O	B3	+5V	Power
A4	D5	I/O	B4	IRQ9	I
A5	D4	I/O	B5	-5V	Power
A6	D3	I/O	B6	DRQ2	I
A7	D2	I/O	B7	-12V	Power
A8	D1	I/O	B8	NOWS#	I
A9	D0	I/O	B9	+12V	Power
A10	CHRDY	I	B10	Gnd SMWTC#	Ground
A11	AEN	O	B11	SMRDC#	O
A12	SA19	I/O	B12	IOWC#	O
A13	SA18	I/O	B13	IORC#	I/O
A14	SA17	I/O	B14	DAK3#	I/O
A15	SA16	I/O	B15	DRQ3	O
A16	SA15	I/O	B16	DAK1#	I
A17	SA14	I/O	B17	DRQ1	O
A18	SA13	I/O	B18	REFRESH#	I
A19	SA12	I/O	B19	BCLK	I/O
A20	SA11	I/O	B20	IRQ7	O
A21	SA10	I/O	B21	IRQ6	I
A22	SA9	I/O	B22	IRQ5	I
A23	SA8	I/O	B23	IRQ4	I
A24	SA7	I/O	B24	IRQ3	I
A25	SA6	I/O	B25	DAK2#	I
A26	SA5	I/O	B26	T-C	O
A27	SA4	I/O	B27	BALE	O
A28	SA3	I/O	B28	+5V	O
A29	SA2	I/O	B29	OSC	Power
A30	SA1	I/O	B30	Gnd	O
A31	SA0	I/O	B31		Ground

I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
C1	SBHE#	I/O	D1	M16#	I
C2	LA23	I/O	D2	IO16#	I
C3	LA22	I/O	D3	IRQ10	I
C4	LA21	I/O	D4	IRQ11	I
C5	LA20	I/O	D5	IRQ12	I
C6	LA19	I/O	D6	IRQ15	I
C7	LA18	I/O	D7	IRQ14	I
C8	LA17	I/O	D8	DAK0#	O
C9	MRDC#	I/O	D9	DRQ0	I
C10	MWTC#	I/O	D10	DAK5#	O
C11	D8	I/O	D11	DRQ5	I
C12	D9	I/O	D12	DAK6#	O
C13	D10	I/O	D13	DRQ6	I
C14	D11	I/O	D14	DAK7#	O
C15	D12	I/O	D15	DRQ7	I
C16	D13	I/O	D16	+5V	Power
C17	D14	I/O	D17	Master16#	I
C18	D15	I/O	D18	Gnd	Ground

ISA BUS SIGNAL DESCRIPTIONS

The following is a description of the ISA Bus signals. All signal lines are TTL-compatible.

AEN (O)

Address Enable (AEN) is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

BALE (O) (Buffered)

Address Latch Enable (BALE) is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with AEN). Microprocessor addresses SA[19::0] are latched with the falling edge of BALE. BALE is forced high during DMA cycles.

BCLK (O)

BCLK is the system clock. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

CHRDY (I)

I/O Channel Ready (CHRDY) is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles. This signal should be held low for no more than 2.5 micro-seconds.

D[15::0] (I/O)

Data signals D[15::0] provide bus bits 15 through 0 for the microprocessor, memory, and I/O devices. D15 is the most-significant bit and D0 is the least-significant bit. All 8-bit devices on the I/O channel should use D[7::0] for communications to the microprocessor. The 16-bit devices will use D[15::0]. To support 8-bit devices, the data on D[15::8] will be gated to D[7::0] during 8-bit transfers to these devices. 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

DAK[7::5]#, DAK[3::0]# (O)

DMA Acknowledge DAK[7::5]# and DAK[3::0]# are used to acknowledge DMA requests DRQ[7::5] and DRQ[3::0]. They are active low.

DRQ[7::5], DRQ[3::0] (I)

DMA Requests DRQ[7::5] and DRQ[3::0] are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritized, with DRQ0 having the highest priority and DRQ7 having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DAK) line goes active. DRQ[3::0] will perform 8-bit DMA transfers; DRQ[7::5] will perform 16-bit transfers.

IO16# (I)

I/O 16-bit Chip Select (IO16#) signals the system board that the present data transfer is a 16-bit, 1 wait-state, I/O cycle. It is derived from an address decode. IO16# is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

IOCHK# (I)

I/O Channel Check (IOCHK#) provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

IORC# (I/O)

I/O Read (IORC#) instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

IOWC# (I/O)

I/O Write (IOWC#) instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

IRQ[15::14], IRQ[12::9], IRQ[7::3] (I)

Interrupt Requests IRQ[15::14], IRQ[12::9] and IRQ[7::3] are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritized, with IRQ[15::14] and IRQ[12::9] having the highest priority (IRQ9 is the highest) and IRQ[7::3] having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine).

LA[23::17] (I/O)

These signals (unlatched) are used to address memory and I/O devices within the system. They give the system up to 16MB of addressability. These signals are valid when BALE is high. LA[23::17] are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by I/O adapters on the falling edge of BALE. These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

M16# (I)

M16# Chip Select signals the system board if the present data transfer is a 1<N>wait-state, 16-bit, memory cycle. It must be derived from the decode of LA[23::17]. M16# should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

Master16# (I)

Master16# is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DAK#. Upon receiving the DAK#, an I/O microprocessor may pull Master16# low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After Master16# is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15<N>microseconds, system memory may be lost because of a lack of refresh.

NOWS# (I)

The No Wait State (NOWS#) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, NOWS# is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, NOWS# should be driven active on system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to a 8-bit device are active on the falling edge of the system clock. NOWS# is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

OSC (O)

Oscillator (OSC) is a high-speed clock with a 70-nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

REFRESH# (I/O)

The REFRESH# signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

RESDRV (O)

Reset Drive (RESDRV) is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SA[19::0] (I/O)

Address bits SA[19::0] are used to address memory and I/O devices within the system. These twenty address lines, in addition to LA[23::17], allow access of up to 16MB of memory. SA[19::0] are gated on the system bus when BALE is high and are latched on the falling edge of BALE. These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

SBHE# (I/O)

System Bus High Enable (SBHE#) indicates a transfer of data on the upper byte of the data bus, D[15::8]. 16-bit devices use SBHE# to condition data bus buffers tied to D[15::8].

SMRDC# (O), MRDC# (I/O)

These signals instruct the memory devices to drive data onto the data bus. SMRDC# is active only when the memory decode is within the low 1MB of memory space. MRDC# is active on all memory read cycles. MRDC# may be driven by any microprocessor or DMA controller in the system. SMRDC is derived from MRDC# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MRDC#, it must have the address lines valid on the bus for one system clock period before driving MRDC# active. Both signals are active low.

SMWTC# (O), MWTC# (I/O)

These signals instruct the memory devices to store the data present on the data bus. SMWTC# is active only when the memory decode is within the low 1MB of the memory space. MWTC# is active on all memory write cycles. MWTC# may be driven by any microprocessor or DMA controller in the system. SMWTC# is derived from MWTC# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MWTC#, it must have the address lines valid on the bus for one system clock period before driving MWTC# active. Both signals are active low.

T-C (O)

Terminal Count (T-C) provides a pulse when the terminal count for any DMA channel is reached.

I/O ADDRESS MAP*

Hex Range	Device
000-01F	DMA Controller 1
020-03F	Interrupt Controller 1, Master
040-05F	Timer
060-06F	8042 (Keyboard)
070-07F	Real-time Clock, NMI (non-maskable interrupt) Mask
080-09F	DMA Page Register
0A0-0BF	Interrupt Controller 2
0C0-0DF	DMA Controller 2
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, Bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

INTERRUPT ASSIGNMENTS*

Interrupt	Description
IRQ0	Timer Output 0
IRQ1	Keyboard (Output Buffer Full)
IRQ2	Interrupt 8 through 15
IRQ3	Serial Port 2
IRQ4	Serial Port 1
IRQ5	Parallel Port 2
IRQ6	Diskette Controller
IRQ7	Parallel Port 1
IRQ8	Real-time Clock Interrupt
IRQ9	Software Redirected to INT 0AH (IRQ2)
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	PS/2 Mouse
IRQ13	Coprocessor
IRQ14	Fixed Disk Controller
IRQ15	Unassigned (may be assigned by the system to the secondary IDE)

* These are typical parameters, which may not reflect your current system.

PCI LOCAL BUS OVERVIEW

The PCI (Peripheral Component Interconnect) Local Bus is a high performance, 32-bit or 64-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between highly integrated peripheral controller components, peripheral add-in boards and processor/memory systems.

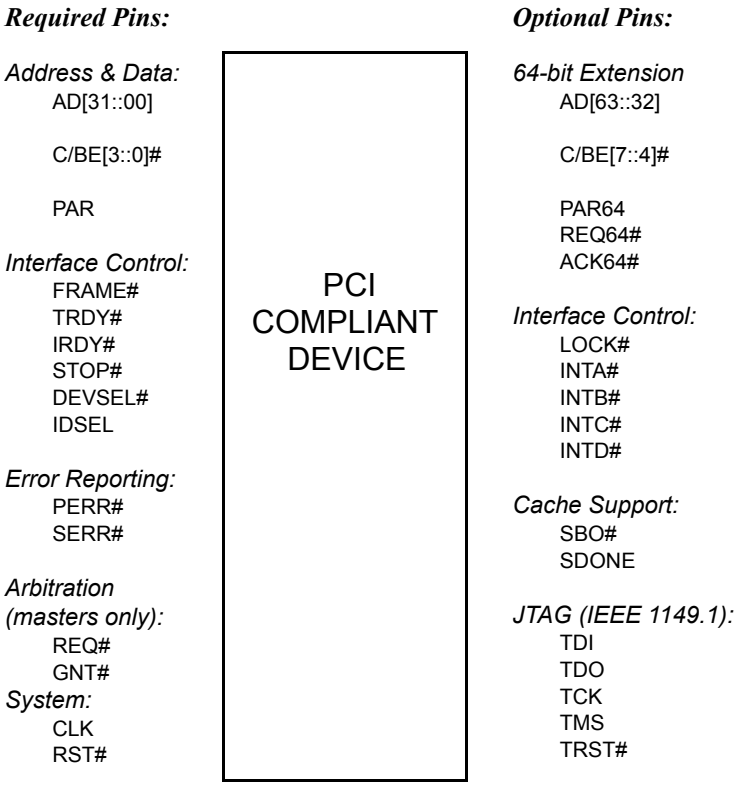
The "local bus" moves peripheral functions with high bandwidth requirements closer to the system's processor bus and can produce substantial performance gains with graphical user interfaces (GUI's) and other high bandwidth functions (i.e., full motion video, SCSI, LAN's, etc.).

The PCI Local Bus accommodates future system requirements and is applicable across multiple platforms and architectures.

The PCI component and add-in card interface is processor independent, enabling an efficient transition to future processor generations, by bridges or by direct integration, and use with multiple processor architectures. Processor independence allows the PCI Local Bus to be optimized for I/O functions, enables concurrent operation of the local bus with the processor/memory subsystem, and accommodates multiple high performance peripherals in addition to graphics. Movement to enhanced video and multimedia displays and other high bandwidth I/O will continue to increase local bus bandwidth requirements. A transparent 64-bit extension of the 32-bit data and address buses is defined, doubling the bus bandwidth and offering forward and backward compatibility of 32-bit (132MB/s peak) and 64-bit (264MB/s peak) PCI Local Bus peripherals.

PCI LOCAL BUS SIGNAL DEFINITION

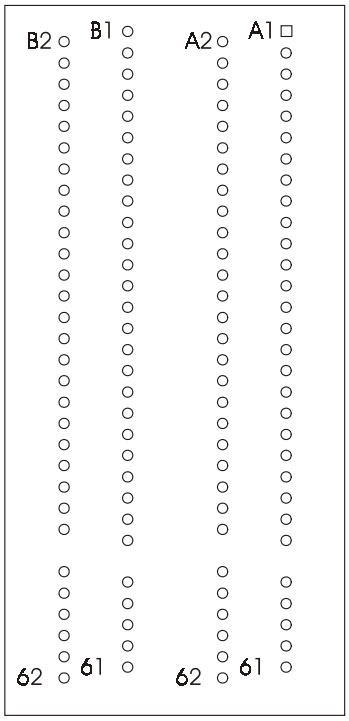
The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for a master to handle data and addressing, interface control, arbitration and system functions. The diagram below shows the pins in functional groups, with required pins on the left side and optional pins on the right side.



PCI Pin List

PCI LOCAL BUS
PIN NUMBERING

Component Side of Board



5-volt/32-bit PCI Connector

PCI LOCAL BUS PIN ASSIGNMENTS

The PCI Local Bus pin assignments shown below are for the PCI option slots on the backplane.

The PCI Local Bus specifies both 5-volt and 3.3-volt signaling environments. The following bus pin assignments are for the 5-volt connector. The 3.3-volt connector bus pin assignments are the same with the following exceptions:

* The pins noted as +V (I/O) are +5 volts or +3.3 volts, depending on which connector is being used.

† Pins B12, B13, A12 and A13 are Gnd (ground) on the 5-volt connector, but are Connector Keys on the 3.3-volt connector.

†† Pin B49 is Gnd (ground) on the 5-volt connector, but is M66EN on the 3.3-volt connector.

††† Pins B50, B51, A50 and A51 are Connectors Keys on the 5-volt connector, but are Gnd (ground) on the 3.3-volt connector.

I/O Pin	Signal Name	I/O Pin	Signal Name
B1	-12V	A1	TRST#
B2	TCK	A2	+12V
B3	Gnd	A3	TMS
B4	TDO	A4	TDI
B5	+5V	A5	+5V
B6	+5V	A6	INTA#
B7	INTB#	A7	INTC#
B8	INTD#	A8	+5V
B9	PRSNT1#	A9	Reserved
B10	Reserved	A10	+V (I/O) *
B11	PRSNT2#	A11	Reserved
B12	Gnd †	A12	Gnd †
B13	Gnd †	A13	Gnd †
B14	Reserved	A14	Reserved
B15	Gnd	A15	RST#
B16	CLK	A16	+V (I/O) *
B17	Gnd	A17	GNT#
B18	REQ#	A18	Gnd
B19	+V (I/O) *	A19	Reserved
B20	AD31	A20	AD30
B21	AD29	A21	+3.3V
B22	Gnd	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	Gnd
B25	+3.3V	A25	AD24
B26	C/BE3#	A26	IDSEL
B27	AD23	A27	+3.3V
B28	Gnd	A28	AD22
B29	AD21	A29	AD20
B30	AD19	A30	Gnd
B31	+3.3V	A31	AD18
B32	AD17	A32	AD16
B33	C/BE2#	A33	+3.3V
B34	Gnd	A34	FRAME#
B35	IRDY#	A35	Gnd

32-bit connector

PCI LOCAL BUS PIN ASSIGNMENTS (CONTINUED)

I/O Pin	Signal Name	I/O Pin	Signal Name	
B36	+3.3V	A36	TRDY#	
B37	DEVSEL#	A37	Gnd	
B38	Gnd	A38	STOP#	
B39	LOCK#	A39	+3.3V	
B40	PERR#	A40	SDONE	
B41	+3.3V	A41	SBO#	
B42	SERR#	A42	Gnd	
B43	+3.3V	A43	PAR	
B44	C/BE1#	A44	AD15	
B45	AD14	A45	+3.3V	
B46	Gnd	A46	AD13	
B47	AD12	A47	AD11	
B48	AD10	A48	Gnd	
B49	Gnd ††	A49	AD9	
B50	Connector Key †††	A50	Connector Key †††	5-volt key
B51	Connector Key †††	A51	Connector Key †††	5-volt key
B52	AD8	A52	C/BE0#	
B53	AD7	A53	+3.3V	
B54	+3.3V	A54	AD6	
B55	AD5	A55	AD4	
B56	AD3	A56	Gnd	
B57	Gnd	A57	AD2	
B58	AD1	A58	AD0	
B59	+V (I/O) *	A59	+V (I/O) *	
B60	ACK64#	A60	REQ64#	
B61	+5V	A61	+5V	
B62	+5V	A62	+5V	32-bit connector end

PCI LOCAL BUS PIN ASSIGNMENTS (CONTINUED)

The following pin assignments apply only to backplanes with 64-bit PCI option slots.

I/O Pin	Signal Name	I/O Pin	Signal Name	
	Connector Key		Connector Key	64-bit spacer
	Connector Key		Connector Key	64-bit spacer
B63	Reserved	A63	Gnd	64-bit connector start
B64	Gnd	A64	C/BE7#	
B65	C/BE6#	A65	C/BE5#	
B66	C/BE4#	A66	+V (I/O) *	
B67	Gnd	A67	PAR64	
B68	AD63	A68	AD62	
B69	AD61	A69	Gnd	
B70	+V (I/O) *	A70	AD60	
B71	AD59	A71	AD58	
B72	AD57	A72	Gnd	
B73	Gnd	A73	AD56	
B74	AD55	A74	AD54	
B75	AD53	A75	+V (I/O) *	
B76	Gnd	A76	AD52	
B77	AD51	A77	AD50	
B78	AD49	A78	Gnd	
B79	+V (I/O) *	A79	AD48	
B80	AD47	A80	AD46	
B81	AD45	A81	Gnd	
B82	Gnd	A82	AD44	
B83	AD43	A83	AD42	
B84	AD41	A84	+V (I/O) *	
B85	Gnd	A85	AD40	
B86	AD39	A86	AD38	
B87	AD37	A87	Gnd	
B88	+V (I/O) *	A88	AD36	
B89	AD35	A89	AD34	
B90	AD33	A90	Gnd	
B91	Gnd	A91	AD32	
B92	Reserved	A92	Reserved	
B93	Reserved	A93	Gnd	64-bit connector end
B94	Gnd	A94	Reserved	

PCI LOCAL BUS SIGNAL DESCRIPTIONS

The PCI Local Bus signals are described below and may be categorized into the following functional groups:

- System Pins
- Address and Data Pins
- Interface Control Pins
- Arbitration Pins (Bus Masters Only)
- Error Reporting Pins
- Interrupt Pins (Optional)
- Cache Support Pins (Optional)
- 64-Bit Bus Extension Pins (Optional)
- JTAG/Boundary Scan Pins (Optional)

A # symbol at the end of a signal name indicates that the active state occurs when the signal is at a low voltage. When the # symbol is absent, the signal is active at a high voltage.

The following are descriptions of the PCI Local Bus signals.

ACK64# (optional)

Acknowledge 64-bit Transfer, when actively driven by the device that has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64bits. ACK64# has the same timing as DEVSEL#.

AD[31::00]

Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. During the address phase, AD[31::00] contain a physical address (32 bits). During data phases, AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb).

AD[63::32] (optional)

Address and Data are multiplexed on the same pins and provide 32additional bits. During an address phase (when using the DAC command and when REQ64# is asserted), the upper 32bits of a 64-bit address are transferred; otherwise, these bits are reserved but are stable and indeterminate. During a data phase, an additional 32bits of data are transferred when REQ64# and ACK64# are both asserted.

C/BE[3::0]#

Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, these pins define the bus command; during the data phase they are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0# applies to byte0 (lsb) and C/BE3# applies to byte 3 (msb).

C/BE[7::4]# (optional)

Bus Command and Byte Enables are multiplexed on the same pins. During an address phase (when using the DAC command and when REQ64# is asserted), the actual bus command is transferred on C/BE[7::4]#; otherwise, these bits are reserved and indeterminate. During a data phase, C/BE[7::4]# are byte enables indicating which byte lanes carry meaningful data when REQ64# and ACK64# are both asserted. C/BE4# applies to byte4 and C/BE7# applies to byte7.

CLK

Clock provides timing for all transactions on PCI and is an input to every PCI device.

DEVSEL#

Device Select, when actively driven, indicates that the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

FRAME#

Cycle Frame is an interface control pin which is driven by the current master to indicate the beginning and duration of an access. When FRAME# is asserted, data transfers continue; when it is deasserted, the transaction is in the final data phase.

GNT#

Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT#.

IDSEL

Initialization Device Select is used as a chip select during configuration read and write transactions.

INTA#, INTB#, INTC#, INTD# (optional)

Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. PCI defines one interrupt for a single function and up to four interrupt lines for a multi-function device or connector.

Interrupt A is used to request an interrupt. For a single function device, only INTA# may be used, while the other three interrupt lines have no meaning.

Interrupt B, Interrupt C and Interrupt D are used to request additional interrupts and only have meaning on a multi-function device.

IRDY#

Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. During a write, IRDY# indicates that valid data is present on AD[31::0]. During a read, it indicates that the master is prepared to accept data.

LOCK#

Lock indicates an operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked.

PAR

Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. The master drives PAR for address and write data phases; the target drives PAR for read data phases.

PAR64 (optional)

Parity Upper DWORD is the even parity bit that protects AD[63::32] and C/BE[7::4]#. The master drives PAR64 for address and write data phases; the target drives PAR64 for read data phases.

PERR#

Parity Error is for the reporting of data parity errors during all PCI transactions except a Special Cycle. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed.

PRSNT1# and PRSNT2#

PRSNT1# and PRSNT2# are related to the connector only, not to other PCI components. They are used for two purposes: indicating that a board is physically present in the slot and providing information about the total power requirements of the board.

REQ#

Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ#.

REQ64# (optional)

Request 64-bit Transfer, when actively driven by the current bus master, indicates it desires to transfer data using 64 bits. REQ64# has the same timing as FRAME#. REQ64# has meaning at the end of reset.

RST#

Reset is used to bring PCI-specific registers, sequencers and signals to a consistent state.

SBO# (optional)

Snoop Backoff is an optional cache support pin which indicates a hit to a modified line when asserted. When SBO# is deasserted and SDONE is asserted, it indicates a "clean" snoop result.

SDONE (optional)

Snoop Done is an optional cache support pin which indicates the status of the snoop for the current access. When deasserted, it indicates the result of the snoop is still pending. When asserted, it indicates the snoop is complete.

SERR#

System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

STOP#

Stop indicates that the current target is requesting the master to stop the current transaction.

TCK (optional)

Test Clock is used to clock state information and test data into and out of the device during operation of the TAP (Test Access Port).

TDI (optional)

Test Data Input is used to serially shift test data and test instructions into the device during TAP (Test Access Port) operation.

TDO (optional)

Test Data Output is used to serially shift test data and test instructions out of the device during TAP (Test Access Port) operation.

TMS (optional)

Test Mode Select is used to control the state of the TAP (Test Access Port) controller in the device.

TRDY#

Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates that the target is prepared to accept data.

TRST# (optional)

Test Reset provides an asynchronous initialization of the TAP controller. This signal is optional in the IEEE Standard Test Access Port and Boundary Scan Architecture.

PICMG EDGE CONNECTOR PIN ASSIGNMENTS

The pin assignments shown below are for the PICMG portion of the edge connector on the processor board. These pin assignments match those of the PICMG connector of the processor slot on the backplane.

I/O Pin	Signal Name	I/O Pin	Signal Name	
B1	-12V	A1	NC	32-bit connector start
B2	NC	A2	+12V	
B3	Gnd	A3	NC	
B4	NC	A4	NC	
B5	+5V	A5	+5V	
B6	+5V	A6	INTA#	
B7	INTB#	A7	INTC#	
B8	INTD#	A8	+5V	
B9	REQ3#	A9	CLKS2	
B10	REQ1#	A10	+5V	
B11	GNT3#	A11	CLKS3	
B12	Gnd	A12	Gnd	
B13	Gnd	A13	Gnd	
B14	CLKS0	A14	GNT1#	
B15	Gnd	A15	RST#	
B16	CLKS1	A16	+5V	
B17	Gnd	A17	GNT0#	
B18	REQ0#	A18	Gnd	
B19	+5V	A19	REQ2#	
B20	AD31	A20	AD30	
B21	AD29	A21	NC	
B22	Gnd	A22	AD28	
B23	AD27	A23	AD26	
B24	AD25	A24	Gnd	
B25	BKPL3.3V	A25	AD24	
B26	C/BE3#	A26	GNT2#	
B27	AD23	A27	NC	
B28	Gnd	A28	AD22	
B29	AD21	A29	AD20	
B30	AD19	A30	Gnd	
B31	NC	A31	AD18	
B32	AD17	A32	AD16	
B33	C/BE2#	A33	NC	
B34	Gnd	A34	FRAME#	
B35	IRDY#	A35	Gnd	
B36	NC	A36	TRDY#	
B37	DEVSEL#	A37	Gnd	
B38	Gnd	A38	STOP#	
B39	LOCK#	A39	NC	
B40	PERR#	A40	SDONE	
B41	NC	A41	SBO#	
B42	SERR#	A42	Gnd	
B43	NC	A43	PAR	
B44	C/BE1#	A44	AD15	
B45	AD14	A45	NC	
B46	Gnd	A46	AD13	
B47	AD12	A47	AD11	
B48	AD10	A48	Gnd	
B49	M66EN	A49	AD9	

PICMG EDGE CONNECTOR PIN ASSIGNMENTS (CONTINUED)

I/O Pin	Signal Name	I/O Pin	Signal Name	
B50	Connector Key	A50	Connector Key	
B51	Connector Key	A51	Connector Key	
B52	AD8	A52	C/BE0#	
B53	AD7	A53	NC	
B54	NC	A54	AD6	
B55	AD5	A55	AD4	
B56	AD3	A56	Gnd	
B57	Gnd	A57	AD2	
B58	AD1	A58	AD0	
B59	+5V	A59	+5V	
B60	ACK64#	A60	REQ64#	
B61	+5V	A61	+5V	
B62	+5V	A62	+5V	32-bit connector end

PICMG EDGE CONNECTOR PIN ASSIGNMENTS (CONTINUED)

The following pin assignments apply only to SBCs with 64-bit PICMG connectors.

I/O Pin	Signal Name	I/O Pin	Signal Name	
	Connector Key		Connector Key	64-bit spacer
	Connector Key		Connector Key	64-bit spacer
B63	NC	A63	Gnd	64-bit connector start
B64	Gnd	A64	C/BE7#	
B65	C/BE6#	A65	C/BE5#	
B66	C/BE4#	A66	+5V	
B67	Gnd	A67	PAR64	
B68	AD63	A68	AD62	
B69	AD61	A69	Gnd	
B70	+5V	A70	AD60	
B71	AD59	A71	AD58	
B72	AD57	A72	Gnd	
B73	Gnd	A73	AD56	
B74	AD55	A74	AD54	
B75	AD53	A75	+5V	
B76	Gnd	A76	AD52	
B77	AD51	A77	AD50	
B78	AD49	A78	Gnd	
B79	+5V	A79	AD48	
B80	AD47	A80	AD46	
B81	AD45	A81	Gnd	
B82	Gnd	A82	AD44	
B83	AD43	A83	AD42	
B84	AD41	A84	+5V	
B85	Gnd	A85	AD40	
B86	AD39	A86	AD38	
B87	AD37	A87	Gnd	
B88	+5V	A88	AD36	
B89	AD35	A89	AD34	
B90	AD33	A90	Gnd	
B91	Gnd	A91	AD32	
B92	NC	A92	NC	
B93	NC	A93	Gnd	
B94	Gnd	A94	NC	64-bit connector end

Chapter 3 System BIOS

BIOS OPERATION

Sections 3 through 7 of this manual describe the operation of the American Megatrends AMIBIOS and the BIOS Setup Utility. Refer to *Running AMIBIOS Setup* later in this chapter for standard Setup screens, options and defaults. The available Setup screens, options and defaults may vary if you have a custom BIOS.

When the system is powered on, AMIBIOS performs the Power-On Self Test (POST) routines. These routines are divided into two phases:

1) **System Test and Initialization**. Test and initialize system boards for normal operations.

2) **System Configuration Verification**. Compare defined configuration with hardware actually installed.

If an error is encountered during the diagnostic tests, the error is reported in one of two different ways. If the error occurs before the display device is initialized, a series of beeps is transmitted. If the error occurs after the display device is initialized, the error message is displayed on the screen. See *BIOS Errors* later in this section for more information on error handling.

The following are some of the Power-On Self Tests (POST's) which are performed when the system is powered on:

- CMOS Checksum Calculation
- Keyboard Controller Test
- CMOS Shutdown Register Test
- 8254 Timer Test
- Memory Refresh Test
- Display Memory Read/Write Test
- Display Type Verification
- Entering Protected Mode
- Memory Size Calculation
- Conventional and Extended Memory Test
- DMA Controller Tests
- Keyboard Test
- System Configuration Verification and Setup

AMIBIOS checks system memory and reports it on both the initial AMIBIOS screen and the AMIBIOS System Configuration screen which appears after POST is completed. AMIBIOS attempts to initialize the peripheral devices and if it detects a fault, the screen displays the error condition(s) which has/have been detected. If no errors are detected, AMIBIOS attempts to load the system from a bootable device, such as a floppy disk or hard disk. Boot order may be specified by the **Boot Device Priority** option on the Boot Setup Menu as described in the *Boot Setup* chapter later in this manual.

Normally, the only POST routine visible on the screen is the memory test. The following screen displays when the system is powered on:

Initial Power-On Screen

You have two options:

- Press **<Del>** to access the BIOS Setup Utility.

  This option allows you to change various system parameters such as date and time, disk drives, etc. The *Running AMIBIOS Setup* section of this manual describes the options available.

  You may be requested to enter a password before gaining access to the BIOS Setup Utility. (See *Password Entry* later in this section.)

  If you enter the correct password or no password is required, the BIOS Setup Utility Main Menu displays. (See *Running AMIBIOS Setup* later in this section.)

- Allow the bootup process to continue without invoking the BIOS Setup Utility.

  In this case, after AMIBIOS loads the system, you may be requested to enter a password. (See *Password Entry* later in this section.)

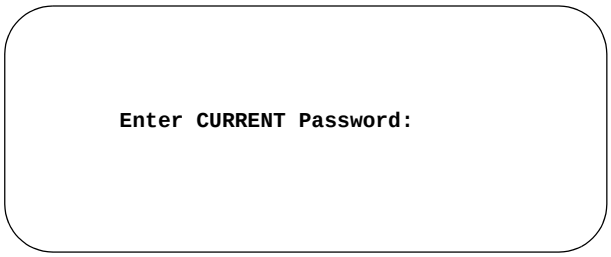
Once the POST routines complete successfully, a screen displays showing the current configuration of your system, including processor type, base and extended memory amounts, floppy and hard drive types, display type and peripheral ports.

Password Entry

The system may be configured so that the user is required to enter a password each time the system boots or whenever an attempt is made to enter the BIOS Setup Utility. The password function may also be disabled so that the password prompt does not appear under any circumstances.

The **Password Check** option in the Security Menu allows you to specify when the password prompt displays: **Always** or only when **Setup** is attempted. This option is available only if the supervisor and/or user password(s) have been established. The supervisor and user passwords may be changed using the **Change Supervisor Password** and **Change User Password** options on the Security Menu. If the passwords are null, the password prompt does not display at any time. See the *Security Setup* section of this chapter for details on setting up passwords.

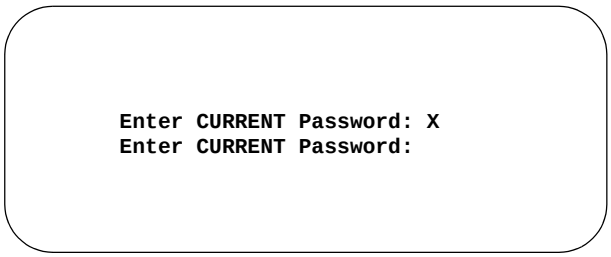
When password checking is enabled, the following password prompt displays:



Type the password and press **<Enter>**.

NOTE: The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the password prompt does not display. To set up passwords, you may use the **Change Supervisor Password** and **Change User Password** options on the Security Menu of the BIOS Setup Utility. (See the *Security Setup* section later in this chapter.)

If an incorrect password is entered, the following screen displays:



You may try again to enter the correct password. If you enter the password incorrectly three times, the system responds in one of two different ways, depending on the value specified in the **Password Check** option on the Security Menu:

1) If the **Password Check** option is set to **Setup**, the system does not let you enter Setup, but does continue the booting process. You must reboot the system manually to retry entering the password.

2) If the **Password Check** option is set to **Always**, the system locks and you must reboot. After rebooting, you will be requested to enter the password.

Once the password has been entered correctly, you are allowed to continue.

BIOS Errors

If an error is encountered during the diagnostic checks performed when the system is powered on, the error is reported in one of two different ways:

1) If the error occurs before the display device is initialized, a series of beeps is transmitted.

2) If the error occurs after the display device is initialized, the screen displays the error message. In the case of a non-fatal error, a prompt to press the **<F1>** key may also appear on the screen.

Explanations of the beep codes and BIOS error messages may be found in *Appendix A - BIOS Messages*.

As the POST routines are performed, test codes are presented on Port 80H. These codes may be helpful as a diagnostic tool and are listed in *Appendix A - BIOS Messages*.

If certain non-fatal error conditions occur, you are requested to run the BIOS Setup Utility. The error messages are followed by this screen:

```
AMIBIOS (C)1999 American Megatrends, Inc.
TRENTON Technology Inc.



Press F1 to Run SETUP
Press F2 to load default values and continue
```

Press **<F1>**. You may be requested to enter a password before gaining access to the BIOS Setup Utility. (See *Password Entry* earlier in this section.)

If you enter the correct password or no password is required, the BIOS Setup Utility Main Menu displays.

RUNNING AMIBIOS SETUP

AMIBIOS Setup keeps a record of system parameters, such as date and time, disk drives, display type and other user-defined parameters. The Setup parameters reside in the Read Only Memory Basic Input/Output System (ROM BIOS) so that they are available each time the system is turned on. The BIOS Setup Utility stores the information in the complementary metal oxide semiconductor (CMOS) memory. When the system is turned off, a backup battery retains system parameters in the CMOS memory.

Each time the system is powered on, it is configured with these values, unless the CMOS has been corrupted or is faulty. The BIOS Setup Utility is resident in the ROM BIOS so that it is available each time the computer is turned on. If, for some reason, the CMOS becomes corrupted, the system is configured with the default values stored in this ROM file.

As soon as the system is turned on, the power-on diagnostic routines check memory, attempt to prepare peripheral devices for action, and offer you the option of pressing **<Del>** to run the BIOS Setup Utility.

If certain non-fatal errors occur during the Power-On Self Test (POST) routines which are run when the system is turned on, you may be prompted to run the BIOS Setup Utility by pressing **<F1>**.

BIOS SETUP UTILITY MAIN MENU

When you press **<F1>** in response to an error message received during the POST routines or when you press the **<Del>** key to enter the BIOS Setup Utility, the following screen displays:

```
                              BIOS SETUP UTILITY
Main    Advanced    Chipset   PCIPnP    Boot   Security   Exit

AMIBIOS Version :            07.00.xx
BIOS Build Date :            11/05/01
BIOS ID         :            0AAXX017

Processor Type  :            Pentium III(tm)
Processor Speed :            866MHz

System Memory   :            256MB



System Time                  [10:22:35]
System Date                  [Mon 01/01/1990]      ←→   Select Screen
                                                   ↑↓   Select Item
                                                   +-   Change Field
                                                   Tab  Select Field
                                                   F1   General Help
                                                   F10  Save and Exit
                                                   ESC  Exit

      vxx.xx (C)Copyright 1985-2000, American Megatrends Inc.
```

BIOS Setup Utility Main Menu

When you display the BIOS Setup Utility Main Menu, the format is similar to the sample shown above. The data displayed on the top portion of the screen details parameters detected by AMIBIOS for your processor board and may not be modified. The system time and date displayed on the bottom portion of the screen may be modified.

BIOS SETUP UTILITY MAIN MENU OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not changed them yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

System Time/System Date

These options allow you to set the correct system time and date. If you do not set these parameters the first time you enter the BIOS Setup Utility, you will receive a "Run SETUP" error message when you boot the system until you set the correct parameters.

The Setup screen displays the system options:

System Time	**[10:22:35]**
System Date	**[Mon 01/01/1990]**

There are three fields for entering the time or date. Use the **<Tab>** key or the **<Enter>** key to move from one field to another and type in the correct value for the field.

If you enter an invalid value in any field, the screen will revert to the previous value when you move to the next field. When you change the value for the month, day or year field, the day of the week changes automatically when you move to the next field.

BIOS SETUP UTILITY OPTIONS

The BIOS Setup Utility allows you to change system parameters to tailor your system to your requirements. Various options which may be changed are listed below. Further explanations of these options and available values may be found in later chapters of this manual, as noted below.

NOTE: Do *not* change the values for any option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

Use the **Right Arrow** key to display the desired menu. The following menus are available:

- Select **Advanced** to make changes to Advanced Setup parameters as described in the *Advanced Setup* chapter of this manual. The following options may be modified:
    - SuperIO Configuration
        - OnBoard Floppy Controller
        - Serial Port1 Address/Serial Port2 Address
        - Parallel Port Address
            - Parallel Port Mode
            - Parallel Port IRQ
    - IDE Configuration
        - OnBoard PCI IDE Controller
        - Primary IDE Master/Primary IDE Slave
          Secondary IDE Master/Secondary IDE Slave
            - Type
            - LBA/Large Mode
            - Block (Multi-Sector Transfer)
            - PIO Mode
            - DMA Mode
            - S.M.A.R.T.
            - 32Bit Data Transfer
            - ARMD Emulation Type

- Hard Disk Write Protect
- ATA(PI) Detect Time Out (Sec)

- Floppy Configuration
  - Floppy A/Floppy B
  - Diskette Write Protect
  - Floppy Drive Seek
- Boot Settings Configuration
  - Quick Boot
  - Quiet Boot
  - AddOn ROM Display Mode
  - Bootup Num-Lock
  - Bootup CPU Speed
  - PS/2 Mouse Support
  - Typematic Rate
  - System Keyboard
  - Primary Display
  - Parity Check
  - Boot To OS/2
  - Wait For ‘F1’ If Error
  - Hit ‘DEL’ Message Display
  - Internal Cache
  - System BIOS Cacheable
- Event Log Configuration
  - Event Logging
  - ECC Event Logging
  - Clear All Event Logs
  - View Event Log
  - Mark All Events as Read
- Remote Access Configuration
  - Remote Access
  - Serial Port Number
  - Serial Port Mode

- Select **Chipset** to make changes to Chipset Setup parameters as described in the *Chipset Setup* chapter of this manual. The following options may be modified:
    - Video and Adapter ROM Shadow
    - Memory Scrubbing
    - Memory Timing Control
        - Act to Deact
        - Act to Read/Write
        - RAS Precharge Time
        - RAS Cycle Time
        - Write to Deact
        - SDRAM CAS Latency
    - ISA IO Cycle Delay
    - Allow Cards to Trap Int19
    - Memory Hole
- Select **PCIPnP** to make changes to PCI Plug and Play Setup parameters as described in the *PCI Plug and Play Setup* chapter of this manual. The following options may be modified:
    - OnBoard LAN1
    - OnBoard LAN2
    - OnBoard VGA
    - OnBoard SCSI
    - Plug & Play O/S
    - Reset Config Data
    - PCI Latency Timer
    - Allocate IRQ to PCI VGA
    - Palette Snooping
    - PCI IDE BusMaster
    - OffBoard PCI/ISA IDE Card
        - OffBoard PCI IDE Primary IRQ
        - OffBoard PCI IDE Secondary
    - USB Function
    - Legacy USB Support
    - IRQs 3, 4, 5, 7, 9, 10, 11, 14 and 15

- DMA Channels 0, 1, 3 5, 6 and 7
- Reserved Memory Size
- Reserved Memory Address

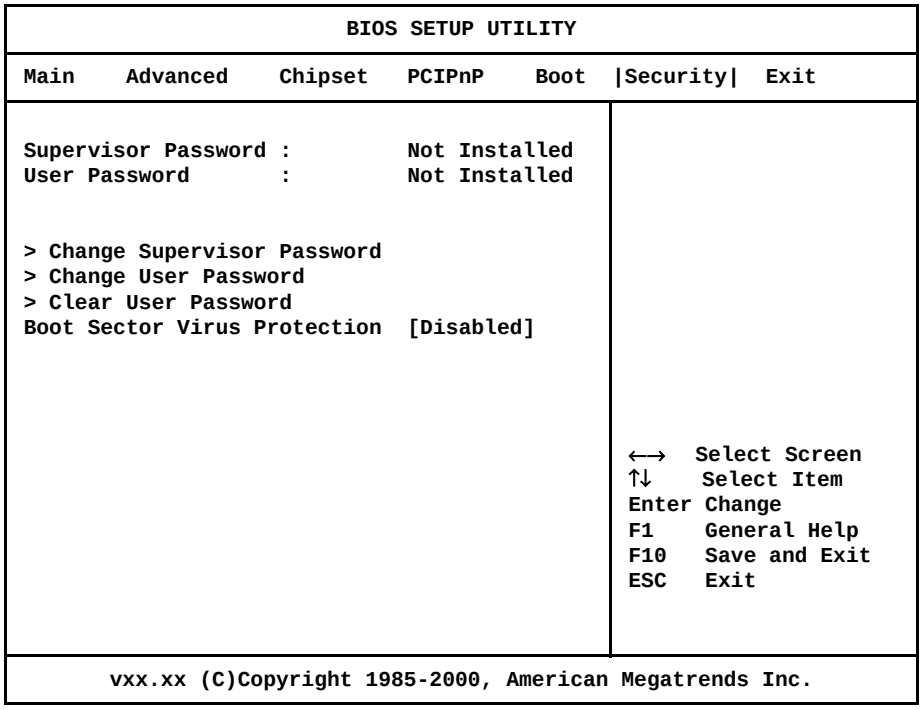
- Select **Boot** to make changes to Boot Setup parameters as described in the *Boot Setup* chapter of this manual. The following options may be modified:
  - Boot Device Priority
  - Hard Disk Drives
  - Removable Devices
  - ATAPI CDROM Drives

- Select **Security** to establish or change the supervisor or user password or to enable boot sector virus protection. These functions are described later in this chapter. The following options may be modified:
  - Change Supervisor Password
    - User Access Level
    - Password Check
  - Change User Password
    - Unattended Start
    - Password Check
  - Clear User Password
  - Boot Sector Virus Protection

- Select **Exit** to save or discard changes you have made to AMIBIOS parameters or to load the Optimal or Failsafe default settings. These functions are described later in this chapter. The following options are available:
  - Exit Saving Changes
  - Exit Discarding Changes
  - Load Optimal Defaults
  - Load Failsafe Defaults
  - Discard Changes

SECURITY SETUP

When you select **Security** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Security Setup Screen

When you display the Security Setup screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>**.

NOTE: The values on this screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

SECURITY SETUP OPTIONS

The Security Setup options allow you to establish, change or clear the supervisor or user password and to enable boot sector virus protection.

The descriptions for the system options listed below show the values as they appear if you have not changed them yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

CHANGE SUPERVISOR PASSWORD

This option allows you to establish a supervisor password, change the current password or disable the password prompt by entering a null password. The password is stored in CMOS RAM.

If you have signed on under the user password, this option is *not* available.

The **Change Supervisor Password** feature can be configured so that a password must be entered each time the system boots or just when a user attempts to enter the BIOS Setup Utility.

NOTE: The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the "Enter CURRENT Password" prompt is bypassed when you boot the system, and you must establish a new password.

If you select the **Change Supervisor Password** option, the following window displays:

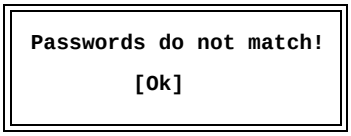
This is the message which displays before you have established a password, or if the last password entered was the null password. If a password has already been established, you are asked to enter the *current* password before being prompted to enter the *new* password.

Type the new password and press **<Enter>**. The password cannot exceed six (6) characters in length. The screen displays an asterisk (*) for each character you type.

After you have entered the new password, the following window displays:

Re-key the new password as described above.

If the password confirmation is miskeyed, AMIBIOS Setup displays the following message:



No retries are permitted; you must restart the procedure.

If the password confirmation is entered correctly, the following message displays:

Press the **<Enter>** key to return to the Security screen. **Installed** displays on the screen next to the **Supervisor Password** option, indicating the password has been accepted. This setting will remain in effect until the supervisor password is either disabled or discarded upon exiting the BIOS Setup Utility.

If you have created a new password, be sure to select **Exit**, then **Exit Saving Changes** to save the password. The password is then stored in CMOS RAM. The next time the system boots, you are prompted for the password.

NOTE: Be sure to keep a record of the new password each time it is changed. If you forget it, use the Password Clear jumper to reset it to the default (null password). See the *Specifications* chapter of this manual for details.

If a password has been established, the following options and their default values are added to the screen:

```
User Access Level          [Full]
Password Check             [Setup]
```

User Access Level

This option allows you to define the level of access the user will have to the system.

The Setup screen displays the system option:

User Access Level [Full]

Four options are available:

- Select **No Access** to prevent user access to the BIOS Setup Utility.
- Select **View Only** to allow access to the BIOS Setup Utility for viewing, but to prevent the user from changing any of the fields.
- Select **Limited** to allow the user to change only a limited number of options, such as Date and Time.
- Select **Full** to allow the user full access to change any option in the BIOS Setup Utility.

Password Check

This option determines when a password is required for access to the system.

The Setup screen displays the system option:

Password Check [Setup]

Two options are available:

- Select **Setup** to have the password prompt appear only when an attempt is made to enter the BIOS Setup Utility program.
- Select **Always** to have the password prompt appear each time the system is powered on.

DISABLING THE SUPERVISOR PASSWORD

To *disable* password checking so that the password prompt does not appear, you may create a null password by selecting the **Change Supervisor Password** function and pressing **<Enter>** without typing in a new password. You will be asked to enter the current password before being allowed to enter the null password. After you press **<Enter>** at the **Enter New Password** prompt, the following message displays:

```
Password uninstalled.
[Ok]
```

CHANGE USER PASSWORD

The **Change User Password** option is similar in functionality to the **Change Supervisor Password** and displays the same messages. If you have signed on under the user password, the **Change Supervisor Password** function is not available for modification.

If a user password has been established, the following options and their default values are added to the screen:

```
Unattended Start          [Disabled]
Password Check            [Setup]
```

Unattended Start

This option specifies whether or not the system should complete the bootup process without requiring a password.

The Setup screen displays the system option:

Unattended Start [Disabled]

Two options are available:

- Select **Disabled** to prevent the system from booting without a password. The keyboard remains locked until a password is entered. A password is required to boot from a diskette.
- Select **Enabled** to allow the system to complete the bootup process without a password.

Password Check

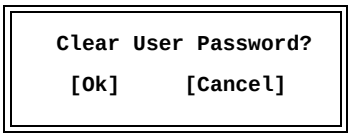
This option determines when a password is required for access to the system.

For details, refer to the description for **Password Check** under the **Change Supervisor Password** heading earlier in this section.

CLEAR USER PASSWORD

This option allows you to clear the user password. It disables the user password by entering a null password.

If you select the **Clear User Password** option, the following window displays:



You have two options:

- Select **Ok** to clear the user password.
- Select **Cancel** to leave the current user password in effect.

BOOT SECTOR VIRUS PROTECTION

This option allows you to request AMIBIOS to issue a warning when any program or virus issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

The Setup screen displays the system option:

Boot Sector Virus Protection [Disabled]

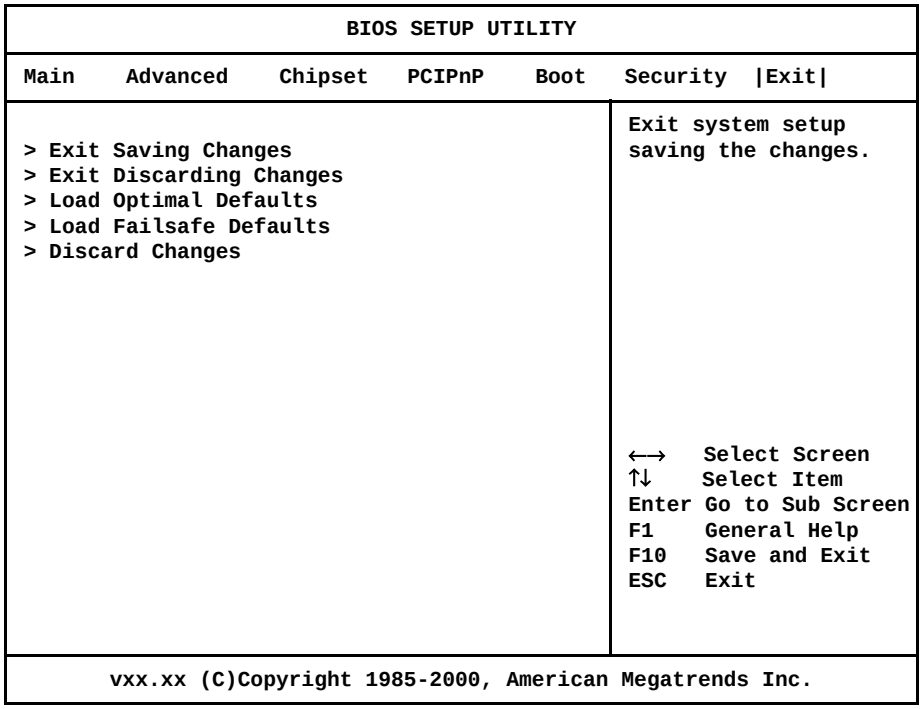
Available options are:

Disabled
Enabled

NOTE: You should *not* enable boot sector virus protection when formatting a hard drive.

EXIT MENU

When you select **Exit** from the BIOS Setup Utility Main Menu, the following screen displays:



Exit Menu Screen

When you display the Exit Menu screen, the format is similar to the sample shown above. Highlight the option you wish to select and press **<Enter>**.

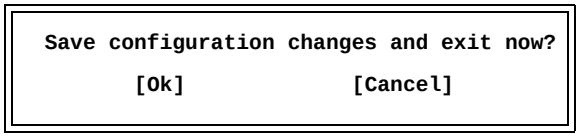
EXIT MENU OPTIONS

When you are running the BIOS Setup Utility program, you may either save or discard changes you have made to AMIBIOS parameters, or you may load the Optimal or Failsafe default settings.

Exit Saving Changes

The features selected and configured in the Setup screens are stored in the CMOS when this option is selected. The CMOS checksum is calculated and written to the CMOS. Control is then passed back to the AMIBIOS and the booting process continues, using the new CMOS values.

If you select the **Exit Saving Changes** option, the following window displays:



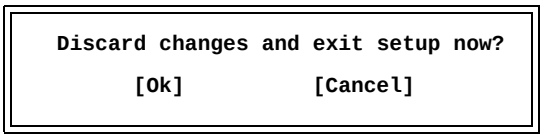
You have two options:

- Select **Ok** to save the system parameters and continue with the booting process.
- Select **Cancel** to return to the BIOS Setup Utility screen.

Exit Discarding Changes

When the **Exit Discarding Changes** option is selected, the BIOS Setup Utility exits *without* saving the changes in the CMOS. Control is then passed back to AMIBIOS and the booting process continues, using the previous CMOS values.

If you select the **Exit Discarding Changes** option, the following window displays:



You have two options:

- Select **Ok** to continue the booting process *without* writing any changes to the CMOS.
- Select **Cancel** to return to the BIOS Setup Utility screen.

Load Optimal or Failsafe Defaults

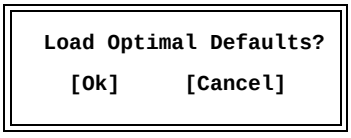
Each AMIBIOS Setup option has two default settings (Optimal and Failsafe). These settings can be applied to all AMIBIOS Setup options when you select the appropriate configuration option from the BIOS Setup Utility Main Menu.

You can use these configuration options to quickly set the system configuration parameters which should provide the best performance characteristics, or you can select a group of settings which have a better chance of working when the system is having configuration-related problems.

Load Optimal Defaults

This option allows you to load the Optimal default settings. These settings are best-case values which should provide the best performance characteristics. If CMOS RAM is corrupted, the Optimal settings are loaded automatically.

If you select the **Load Optimal Defaults** option, the following window displays:



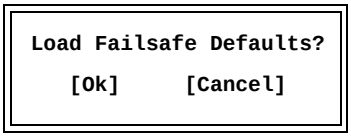
You have two options:

- Select **Ok** to load the Optimal default settings.
- Select **Cancel** to leave the current values in effect.

Load Failsafe Defaults

This option allows you to load the Failsafe default settings when you cannot boot your computer successfully. These settings are more likely to configure a workable computer. They may not provide optimal performance, but are the most stable settings. You may use this option as a diagnostic aid if your system is behaving erratically. Select the Failsafe settings and then try to diagnose the problem after the computer boots.

If you select the **Load Failsafe Defaults** option, the following window displays:



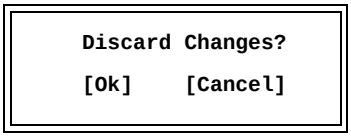
You have two options:

- Select **Ok** to load the Failsafe default settings.
- Select **Cancel** to leave the current values in effect.

Discard Changes

When the **Discard Changes** option is selected, the BIOS Setup Utility resets any parameters you have changed back to the values at which they were set when you entered the Setup Utility. Control is then passed back to the BIOS Setup Utility screen.

If you select the **Discard Changes** option, the following window displays:



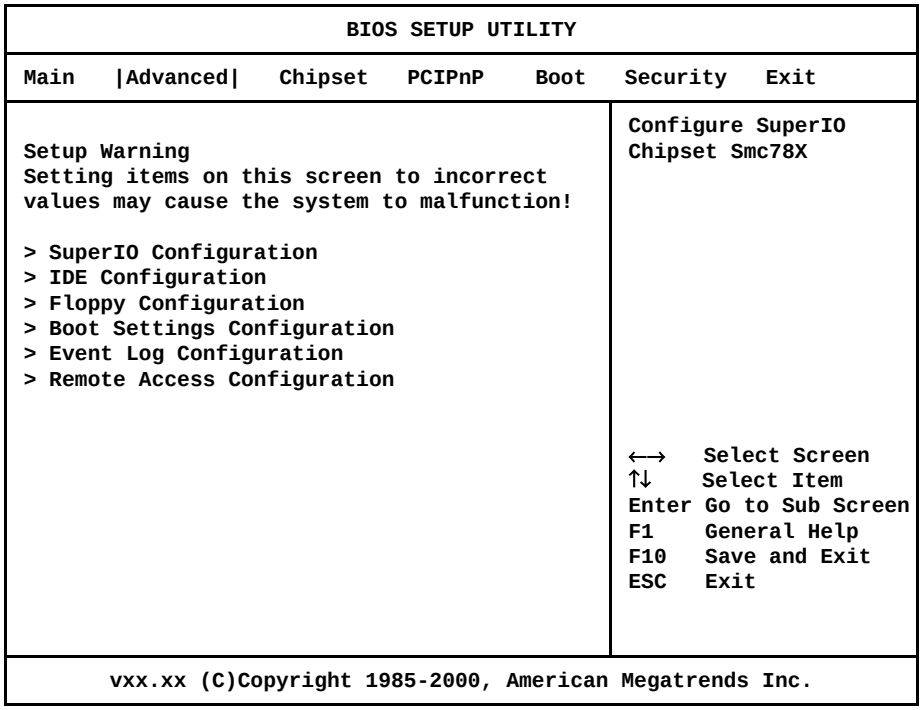
You have two options:

- Select **Ok** to reset any parameters you have changed back to the values at which they were set when you entered the BIOS Setup Utility. This option then returns you to the BIOS Setup Utility screen.
- Select **Cancel** to return to the BIOS Setup Utility screen *without* discarding any changes you have made.

Chapter 4 Advanced Setup

ADVANCED SETUP

When you select **Advanced** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Advanced Setup Screen

When you display the Advanced Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Advanced Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

NOTE: The values on the Advanced Setup subscreens do not necessarily reflect the values appropriate for your SBC. Refer to the explanations following each screen for specific instructions about entering correct information.

ADVANCED SETUP OPTIONS

NOTE: Do *not* change the values for any Advanced Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

SuperIO Configuration

The options on the **SuperIO Configuration** subscreen allow you to set up or modify parameters for your on-board peripherals. The following options may be modified:

- OnBoard Floppy Controller
- Serial Port1 Address/Serial Port2 Address
- Parallel Port Address
    - Parallel Port Mode
    - Parallel Port IRQ

IDE Configuration

The options on the **IDE Configuration** subscreens allow you to set up or modify parameters for your IDE controller and hard disk drive(s). The following options may be modified:

- OnBoard PCI IDE Controller
- Primary IDE Master/Primary IDE Slave
    - Type
    - LBA/Large Mode
    - Block (Multi-Sector Transfer)
    - PIO Mode
    - DMA Mode
    - S.M.A.R.T.
    - 32Bit Data Transfer
    - ARMD Emulation Type
- Secondary IDE Master/Secondary IDE Slave
    - (see options above)
- Hard Disk Write Protect
- ATA(PI) Detect Time Out (Sec)

Floppy Configuration

The options on the **Floppy Configuration** subscreen allow you to set up or modify parameters for your floppy disk drive(s). The following options may be modified:

- Floppy A/Floppy B
- Diskette Write Protect
- Floppy Drive Seek

Boot Settings Configuration

The options on the **Boot Settings Configuration** subscreen allow you to set up or modify parameters for boot procedures. The following options may be modified:

- Quick Boot
- Quiet Boot
- AddOn ROM Display Mode
- Bootup Num-Lock
- Bootup CPU Speed
- PS/2 Mouse Support
- Typematic Rate
- System Keyboard
- Primary Display
- Parity Check
- Boot To OS/2
- Wait For 'F1' If Error
- Hit 'DEL' Message Display
- Internal Cache
- System BIOS Cacheable

Event Log Configuration

The options on the **Event Log Configuration** subscreen allow you to set up or modify parameters for using the event log, which allows you to log errors and other events which occur in the system. The following options may be modified:

- Event Logging
- ECC Event Logging
- Clear All Event Logs

Remote Access Configuration

The options on the **Remote Access Configuration** subscreen allow you to set up or modify parameters for configuring remote access type and parameters. The following options may be modified:

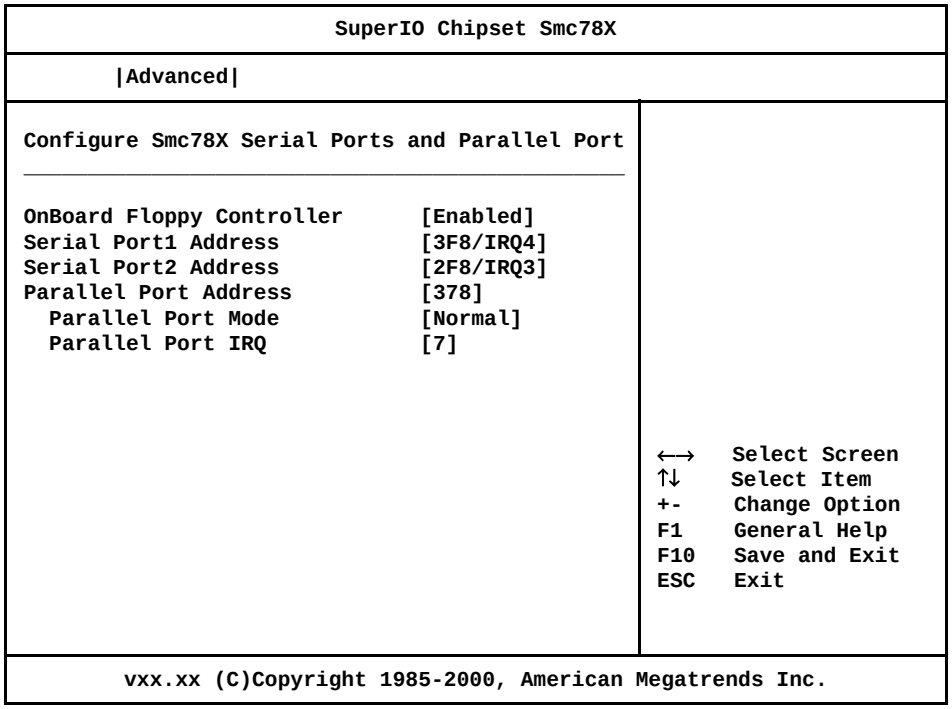
- Remote Access
- Serial Port Number
- Serial Port Mode

Saving and Exiting

When you have made all desired changes to **Advanced Setup**, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

SUPERIO CONFIGURATION

When you select **SuperIO Configuration** from the Advanced Setup Menu, the following Setup screen displays:



SuperIO Configuration Screen

When you display the SuperIO Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

SUPERIO CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

OnBoard Floppy Controller

The on-board floppy drive controller may be enabled or disabled using this option.

The Setup screen displays the system option:

OnBoard Floppy Controller [Enabled]

Available options are:

Disabled
Enabled

Serial Port1 Address/Serial Port2 Address

Each of these options enables the specified serial port on the SBC and establishes the base I/O address and the number of the interrupt request for the port.

The Setup screen displays the system option:

Serial Port1 Address	**[3F8/IRQ4]**
Serial Port2 Address	**[2F8/IRQ3]**

Available options are:

Disabled
3F8/IRQ4
3E8/IRQ4
2F8/IRQ3
2E8/IRQ3

NOTE: The values available for each on-board serial port may vary, depending on the setting previously selected for the other on-board serial port and any off-board serial ports. If an I/O address is assigned to another serial port, AMIBIOS automatically omits that address from the values available.

If the system has off-board serial ports which are configured to specific starting I/O ports via jumper settings, AMIBIOS configures the on-board serial ports to avoid conflicts.

AMIBIOS checks the ISA Bus for serial ports. Any off-board serial ports found on the ISA Bus are left at their assigned addresses. Serial Port1, the first on-board serial port, is configured with the first available address and Serial Port2, the second on-board serial port, is configured with the next available address. The default address assignment order is 3F8H, 2F8H, 3E8H, 2E8H. Note that this same assignment order is used by AMIBIOS to place the active serial port addresses in lower memory (BIOS data area) for configuration as logical COM devices.

For example, if there is one off-board serial port on the ISA Bus and its address is set to 2F8H, Serial Port1 is assigned address 3F8H and Serial Port2 is assigned address 3E8H. Configuration is then as follows:

COM1 - Serial Port1 (at 3F8H)
COM2 - off-board serial port (at 2F8H)
COM3 - Serial Port2 (at 3E8H)

Parallel Port Address

This option enables the parallel port on the SBC and establishes the base I/O address for the port.

The Setup screen displays the system option:

Parallel Port Address	**[378]**

Available options are:

Disabled
378
278
3BC

AMIBIOS checks the ISA Bus for off-board parallel ports. Any parallel ports found on the ISA Bus are left at their assigned addresses. The on-board Parallel Port is automatically configured with the first available address not used by an off-board parallel port.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes which adhere to the IEEE P1284 specifications.

The Setup screen displays the system option:

Parallel Port Mode [Normal]

Three options are available:

- Select **Normal** to use normal parallel port mode.
- Select **EPP** to allow the parallel port to be used with devices which adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
- Select **ECP** to allow the parallel port to be used with devices which adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve transfer rates of approximately 2.5MB/second. ECP provides symmetric bidirectional communication.

Parallel Port IRQ

This option specifies the interrupt request (IRQ) which is used by the parallel port.

The Setup screen displays the system option:

Parallel Port IRQ [7]

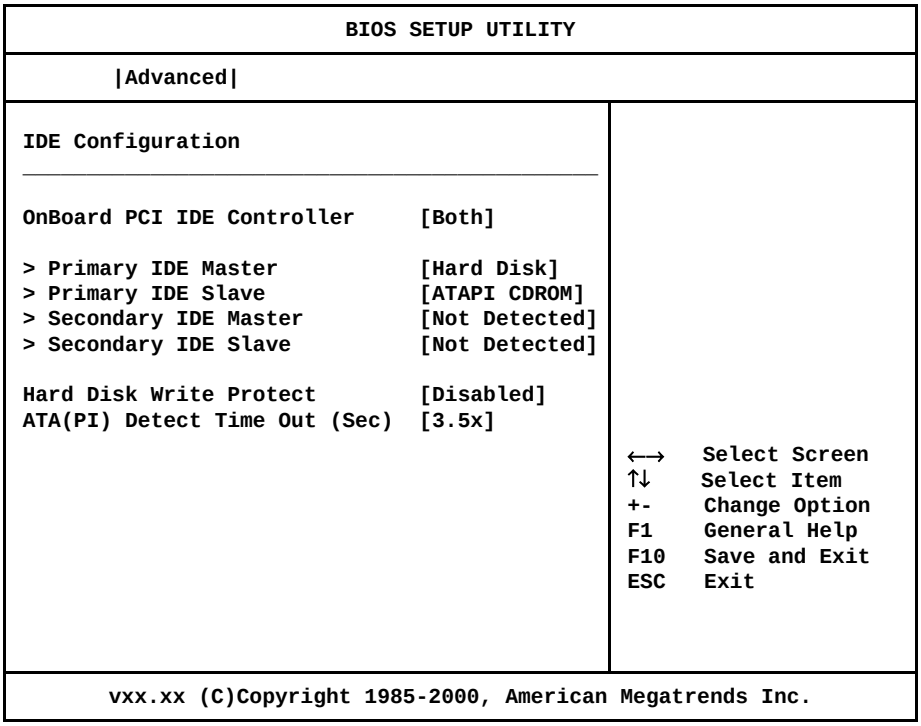
Available options are:

5
7

This page intentionally left blank.

IDE CONFIGURATION

When you select **IDE Configuration** from the Advanced Setup Menu, the following Setup screen displays:



IDE Configuration Screen

When you display the IDE Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

Some of the options on this screen allow you to continue to subscreens designed to change parameters for that particular option. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

IDE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

OnBoard PCI IDE Controller

This option specifies whether or not the on-board integrated drive electronics (IDE) controllers are to be used.

The Setup screen displays the system option:

OnBoard PCI IDE Controller [Both]

Available options are:

Disabled
Both

Primary IDE Master/Primary IDE Slave
Secondary IDE Master/Secondary IDE Slave

The SBC has an enhanced IDE (EIDE) interface which can support up to four IDE disk drives through a primary and secondary controller in a master/slave configuration. This EIDE interface allows disk drives greater than 528MB to be used. Each of the four drives may be a different type.

Devices attached to the primary and secondary controllers are detected automatically by AMIBIOS and displayed on the IDE Configuration screen.

The Setup screen displays the system options:

Primary IDE Master [Hard Disk]
Primary IDE Slave [ATAPI CDROM]

Secondary IDE Master [Not Detected]
Secondary IDE Slave [Not Detected]

To view and/or change parameters for any IDE device, press **<Enter>** to proceed to the IDE Device Setup screen, which is described later in this section.

Hard Disk Write Protect

This option allows you to disable or enable device write protection. Write protection will be effective only if the device is accessed through the BIOS.

The Setup screen displays the system option:

Hard Disk Write Protect [Disabled]

Available options are:

Disabled
Enabled

ATA(PI) Detect Time Out (Sec)

This option allows you to select the time-out value (in seconds) for detecting an ATA/ ATAPI device.

The Setup screen displays the system option:

ATA(PI) Detect Time Out (Sec) [3.5x]

Available options are:

0
5
10
15
2.0x
2.5x
3.0x
3.5x

This page intentionally left blank.

IDE DEVICE SETUP

When you select one of the IDE devices from the **IDE Configuration** screen, a Setup screen similar to the following displays:

```
                        BIOS SETUP UTILITY
       |Advanced|
Primary IDE Master                                  |
-------------------------------------               |
Device    :                  Hard Disk              |
Vendor    :                  ST33210A               |
Size      :                  3.2GB                  |
LBA Mode  :                  Supported              |
Block Mode:                  16Sectors              |
PIO Mode  :                  4                      |
Async DMA :                  MultiWord DMA-2        |
Ultra DMA :                  Ultra DMA-2            |
S.M.A.R.T.:                  Supported              |
-------------------------------------               |
Type                         [Auto}                 |
LBA/Large Mode               [Auto]                 | ←→  Select Screen
Block (Multi-Sector Transfer) [Auto]                | ↑↓  Select Item
PIO Mode                     [Auto]                 | +-  Change Option
DMA Mode                     [Auto]                 | F1  General Help
S.M.A.R.T.                   [Auto]                 | F10 Save and Exit
32Bit Data Transfer          [Disabled]             | ESC Exit
ARMD Emulation Type          [Auto]                 |
       vxx.xx (C)Copyright 1985-2000, American Megatrends Inc.
```

IDE Device Screen

When you display the IDE Device subscreen, the format is similar to the sample shown above. The data displayed on the top portion of the screen details the parameters detected by AMIBIOS for the specified device and may not be modified. The data displayed on the bottom portion of the screen may be modified.

The drive information which displays the first time the BIOS Setup Utility is run indicates the drive(s) on your system which AMIBIOS detected upon initial bootup.

IDE DEVICE SETUP OPTIONS

The following options are available for each of the four IDE devices on the primary and secondary IDE controllers:

Type

This option allows you to specify what type of device is on the IDE controller.

The Setup screen displays the system option:

Type [Auto]

Available options are:

Auto
Not Installed
CDROM
ARMD

If **Not Installed** is selected, the other options on the bottom portion of this screen do not display. If **CDROM** is selected, the **ARMD Emulation Type** option is not available.

LBA/Large Mode

This option allows you to enable IDE LBA (Logical Block Addressing) Mode for the specified IDE drive. Data is accessed by block addresses rather than by the traditional cylinder-head-sector format. This allows you to use drives larger than 528MB.

The Setup screen displays the system option:

LBA/Large Mode [Auto]

Two options are available:

- Select **Auto** to enable LBA mode and translate the physical parameters of the drive to logical parameters. LBA Mode must be supported by the drive and the drive must have been formatted with LBA Mode enabled.
- Select **Disabled** to have AMIBIOS use the physical parameters of the hard disk and do no translation to logical parameters. The operating system which uses the parameter table will then see only 528MB of hard disk space even if the drive contains more than 528MB.

Block (Multi-Sector Transfer) Mode

This option supports transfer of multiple sectors to and from the specified IDE drive. Block mode boosts IDE drive performance by increasing the amount of data transferred during an interrupt.

If **Block Mode** is set to **Disabled**, data transfers to and from the device occur one sector at a time.

The Setup screen displays the system option:

Block (Multi-Sector Transfer) [Auto]

Available options are:

Disabled
Auto

PIO Mode

IDE Programmed I/O (PIO) Mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

Set the **PIO Mode** option to **Auto** to have AMIBIOS select the PIO mode used by the IDE drive being configured. If you select a specific value for the PIO mode, you must make *absolutely* certain that you are selecting the PIO mode supported by the IDE drive being configured.

The Setup screen displays the system option:

PIO Mode [Auto]

Available options are:

Auto
0
1
2
3
4

DMA Mode

This option allows you to select DMA Mode for the device.

The Setup screen displays the system option:

DMA Mode [Auto]

Available options are:

Auto	
SWDMA0	(SingleWord DMA 0 - 2)
SWDMA1	
SWDMA2	
MWDMA0	(MultiWord DMA 0 - 2)
MWDMA1	
MWDMA2	
UDMA0	(UltraDMA 0 - 4)
UDMA1	
UDMA2	
UDMA3	
UDMA4	

S.M.A.R.T.

This option allows AMIBIOS to use the SMART (Self-Monitoring Analysis and Reporting Technology) protocol for reporting server system information over a network.

The Setup screen displays the system option:

S.M.A.R.T. [Auto]

Available options are:

Auto
Disabled
Enabled

32Bit Data Transfer

Hard disk drives connected to the SBC via the ISA Bus transfer data 16 bits at a time. An IDE drive on the PCI Local Bus can use a 32-bit data path.

If the **32Bit Data Transfer** parameter is set to **Enabled**, AMIBIOS enables 32-bit data transfers. If the host controller does not support 32-bit transfer, this feature *must* be set to **Disabled**.

The Setup screen displays the system option:

32Bit Data Transfer [Disabled]

Available options are:

Disabled
Enabled

ARMD Emulation Type

This option specifies the type of ARMD (ATAPI Removable Media Device) emulation used for a non-disk device attached to the specified IDE device.

If the option is set to **Auto**, AMIBIOS automatically determines the proper emulation type and will support particular storage devices with ATAPI interface.

If **CDROM** is selected in the **Type** field, this option is not available for modification.

The Setup screen displays the system options:

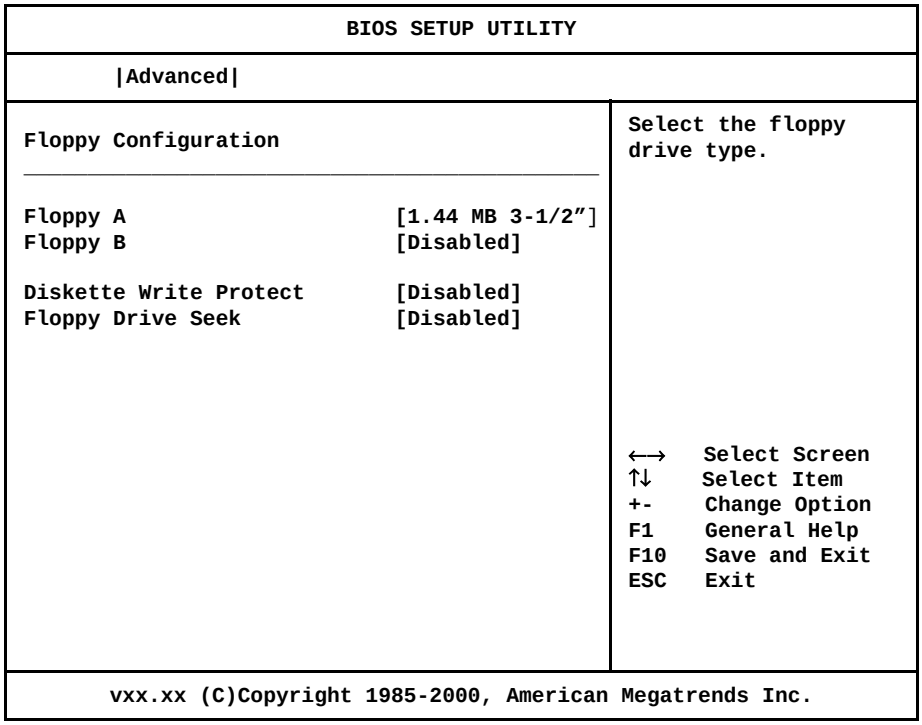
ARMD Emulation Type [Auto]

Available options are:

Auto
Floppy
Hard Disk

FLOPPY CONFIGURATION

When you select **Floppy Configuration** from the Advanced Setup Menu, the following Setup screen displays:



Floppy Configuration Screen

When you display the Floppy Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

The drive information which displays the first time the BIOS Setup Utility is run indicates the drive(s) on your system which AMIBIOS detected upon initial bootup.

FLOPPY CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Floppy A/Floppy B

The floppy drive(s) in your system can be configured using these options. The **Disabled** option can be used for diskless workstations.

The Setup screen displays the system options:

Floppy A	**[1.44 MB 3-1/2"]**
Floppy B	**[Disabled]**

Available options are:

Disabled
360 KB 5-1/4"
1.2 MB 5-1/4"
720 KB 3-1/2"
1.44MB 3-1/2"
2.88MB 3-1/2"

Diskette Write Protect

This option allows you to disable or enable device write protection. Write protection will be effective only if the device is accessed through the BIOS.

The Setup screen displays the system option:

Diskette Write Protect [Disabled]

Available options are:

Disabled
Enabled

Floppy Drive Seek

This option causes the system to have the floppy drive(s) seek during bootup. The default for this option is **Disabled** to allow a fast boot and to decrease the possibility of damage to the heads.

The Setup screen displays the system option:

Floppy Drive Seek [Disabled]

Available options are:

Disabled
Enabled

BOOT SETTINGS CONFIGURATION

When you select **Boot Settings Configuration** from the Advanced Setup Menu, the following Setup screen displays:

```
                        BIOS SETUP UTILITY
       |Advanced|
Boot Settings Configuration                    | Allows BIOS to skip
                                               | certain tests while
                                               | booting. This will
Quick Boot                      [Disabled]     | decrease the time
Quiet Boot                      [Disabled]     | needed to boot the
AddOn ROM Display Mode          [Force BIOS]   | system.
                                               |
BootUp Num-Lock                 [On]           |
BootUp CPU Speed                [High]         |
PS/2 Mouse Support              [Enabled]      |
Typematic Rate                  [Fast]         |
System Keyboard                 [Present]      | ←→  Select Screen
Primary Display                 [VGA/EGA]      | ↑↓  Select Item
Parity Check                    [Enabled]      | +-  Change Option
Boot To OS/2                    [No]           | F1  General Help
Wait For 'F1' If Error          [Enabled]      | F10 Save and Exit
Hit 'DEL' Message Display       [Enabled]      | ESC Exit
Internal Cache                  [Write-Back]   |
System BIOS Cacheable           [Enabled]      |
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```

Boot Settings Configuration Screen

When you display the Boot Settings Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

BOOT SETTINGS CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Quick Boot

This option allows you to have the AMIBIOS boot quickly when the computer is powered on or go through more complete testing. If you set the **Quick Boot** option to **Enabled**, the BIOS skips certain tests while booting and decreases the time needed to boot the system.

The Setup screen displays the system option:

Quick Boot **[Disabled]**

Available options are:

Disabled
Enabled

Quiet Boot

This option specifies what will be displayed on the screen while the system is performing the POST routines when the computer is powered on or a soft reboot is performed.

The Setup screen displays the system option:

Quiet Boot [Disabled]

Two options are available:

- Select **Disabled** to display normal POST messages.
- Select **Enabled** to display the OEM logo instead of the POST messages.

AddOn ROM Display Mode

This option specifies the system display mode which is set at the time the AMIBIOS post routines initialize an optional option ROM.

The Setup screen displays the system option:

AddOn ROM Display Mode [Force BIOS]

Two options are available:

- Select **Force BIOS** to use the display mode currently being used by AMIBIOS.
- Select **Keep Current** to use the current display mode.

BootUp Num-Lock

This option enables you to turn off the Num-Lock option on the enhanced keyboard when the system is powered on. If Num-Lock is turned off, the arrow keys on the numeric keypad can be used, as well as the other set of arrow keys on the enhanced keyboard.

The Setup screen displays the system option:

BootUp Num-Lock [On]

Available options are:

Off
On

BootUp CPU Speed

The Setup screen displays the system option:

BootUp CPU Speed [High]

Available options are:

Low
High

PS/2 Mouse Support

This option indicates whether or not a PS/2-type mouse is supported.

The Setup screen displays the system option:

PS/2 Mouse Support [Enabled]

Available options are:

Disabled
Enabled

Typematic Rate

The Setup screen displays the system option:

Typematic Rate [Fast]

Available options are:

Slow
Fast

System Keyboard

This option indicates whether or not a keyboard is attached to the computer.

The Setup screen displays the system option:

System Keyboard [Present]

Available options are:

Absent
Present

Primary Display

This option specifies the type of display monitor in the system. The **Absent** option can be used for network file servers.

The Setup screen displays the system option:

Primary Display **[VGA/EGA]**

Available options are:

Absent
VGA/EGA
Color 40 x 25
Color 80 x 25
Monochrome

Parity Check

This option allows you to enable parity checking of all system memory.

The Setup screen displays the system option:

Parity Check **[Enabled]**

Available options are:

Disabled
Enabled

Boot To OS/2

This option should be set to **Yes** if you are running the IBM OS/2 operating system and using more than 64MB of system memory on the SBC.

The Setup screen displays the system option:

Boot To OS/2 **[No]**

Available options are:

No
Yes

Wait For 'F1' If Error

Before the system boots up, the AMIBIOS executes the Power-On Self Test (POST) routines, a series of system diagnostic routines. If any of these tests fail but the system can still function, a non-fatal error has occurred. The AMIBIOS responds with an appropriate error message followed by:

Press F1 to RESUME

If this option is set to **Disabled**, a non-fatal error does not generate the "Press F1 to RESUME" message. The AMIBIOS still displays the appropriate message, but continues the booting process without waiting for the **<F1>** key to be pressed. This eliminates the need for any user response to a non-fatal error condition message. Non-fatal error messages are listed in *Appendix A - BIOS Messages*.

The Setup screen displays the system option:

Wait For 'F1' If Error [Enabled]

Available options are:

Disabled
Enabled

Hit 'DEL' Message Display

The "Hit DEL to run Setup" message displays when the system boots up. Disabling this option prevents the message from displaying.

The Setup screen displays the system option:

Hit 'DEL' Message Display [Enabled]

Available options are:

Disabled
Enabled

Internal Cache

This option specifies the caching algorithm used for L1 internal cache memory.

The Setup screen displays the system option:

Internal Cache [Write-Back]

Four options are available:

- Select **Disabled** to disable both L1 internal cache memory on the SBC and L2 secondary cache memory.
- Select **Write-Thru** to use the write-through caching algorithm.
- Select **Write-Back** to use the write-back caching algorithm.
- Select **Reserved**.

System BIOS Cacheable

The System BIOS, which is in the F000H memory segment, is automatically shadowed to RAM for faster execution. This option indicates that this memory segment can be read from or written to cache memory.

The Setup screen displays the system option:

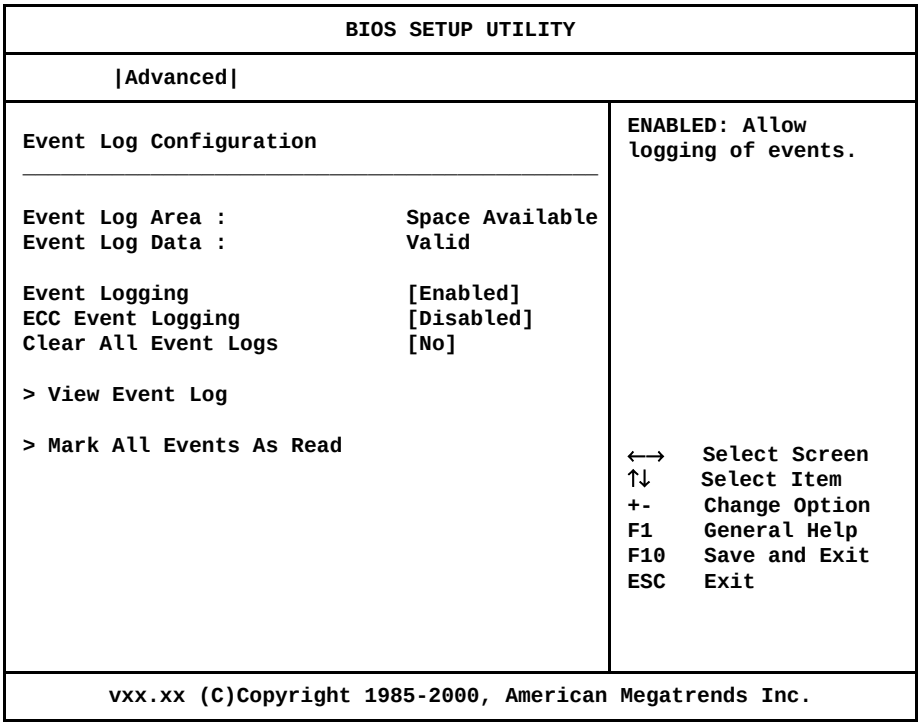
System BIOS Cacheable [Enabled]

Available options are:

Disabled
Enabled

EVENT LOG CONFIGURATION

When you select **Event Log Configuration** from the Advanced Setup Menu, the following Setup screen displays:



Event Log Configuration Screen

When you display the Event Log Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press <**Enter**> again to accept the highlighted value.

EVENT LOG CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Event Logging

This option allows logging of events.

The Setup screen displays the system option:

Event Logging [Enabled]

Available options are:

Disabled
Enabled

ECC Event Logging

This option allows logging of error checking and correction (ECC) events.

The Setup screen displays the system option:

ECC Event Logging [Disabled]

Available options are:

Disabled
Enabled

Clear All Event Logs

This option specifies whether or not the event logs should be cleared on the next boot.

The Setup screen displays the system option:

Clear All Event Logs [No]

Available options are:

No
Yes

View Event Log

When you select this option, a window similar to the following displays showing events which have been logged:

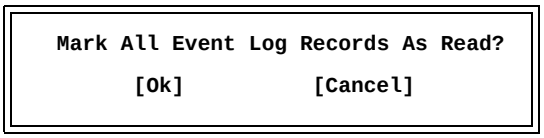
```
        View Event Log

Pre-Boot Error:
  CMOS Checksum Error
Pre-Boot Error:
  CMOS System Options Not Set
Pre-Boot Error:
  CMOS Checksum Error
```

When you have finished viewing the Event Log, press **<Esc>** to continue.

Mark All Events As Read

After you have reviewed the events in the event log, you may select this option, which allows you to mark all event log entries as having been read.

The following window displays:

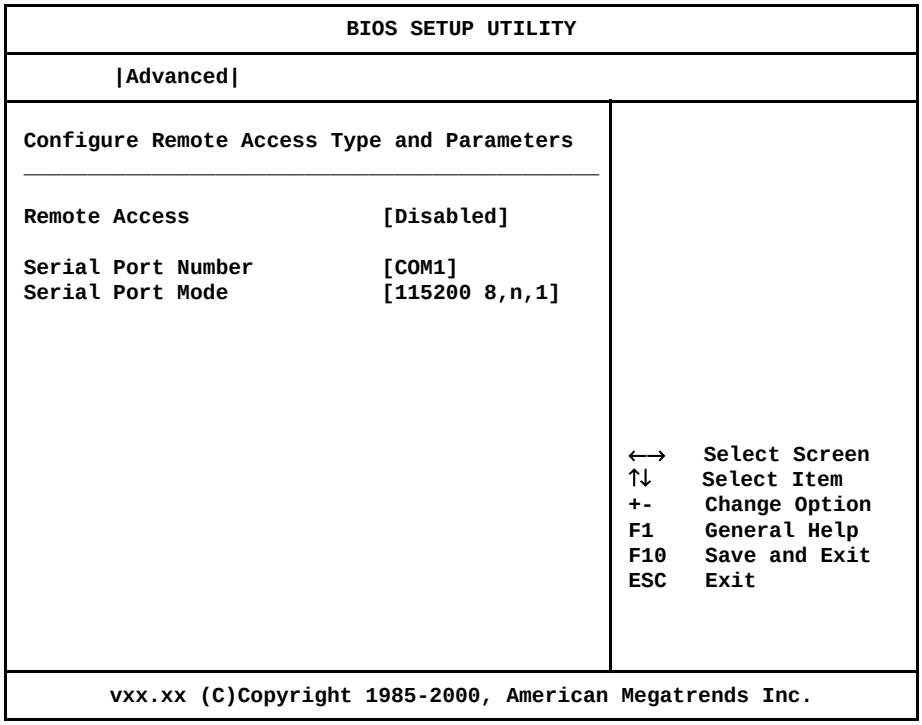


Selecting **Ok** marks *all* entries currently in the event log file as having been read. The next time you select the **View Event Log** option, only the new, unmarked events are displayed.

This page intentionally left blank.

REMOTE ACCESS CONFIGURATION

When you select **Remote Access Configuration** from the Advanced Setup Menu, the following Setup screen displays:



Remote Access Configuration Screen

When you display the Remote Access Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

REMOTE ACCESS CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Remote Access

This option allows you to use a terminal connected to the serial port of the SBC to control changes to the BIOS settings.

The Setup screen displays the system option:

Remote Access [Disabled]

Available options are:

Disabled
Serial (ANSI)

If this option is set to **Disabled**, the **Serial Port Number** and **Serial Port Mode** options are not available.

Serial Port Number

This option specifies the serial port on which remote access is to be enabled.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Serial Port Number [COM1]

Available options are:

COM1
COM2

Serial Port Mode

This option specifies settings for the serial port on which remote access is enabled. The settings indicate baud rate, eight bits per character, no parity and one stop bit.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Serial Port Mode [115200 8,n,1]

Available options are:

9600 8,n,1
19200 8,n,1
57600 8,n,1
115200 8,n,1

Chapter 5 Chipset Setup

CHIPSET SETUP

When you select **Chipset** from the BIOS Setup Utility Main Menu, the following Setup screen displays:

```
                        BIOS SETUP UTILITY
Main    Advanced   |Chipset|  PCIPnP    Boot   Security   Exit

C000, 16k Shadow            [Cached]
C400, 16k Shadow            [Cached]
C800, 16k Shadow            [Disabled]
CC00, 16k Shadow            [Disabled]
D000, 16k Shadow            [Disabled]
D400, 16k Shadow            [Disabled]
D800, 16k Shadow            [Disabled]
DC00, 16k Shadow            [Disabled]
Memory Scrubbing            [Disabled]
Memory Timing Control       [Auto]
ISA IO Cycle Delay          [FULL Delay]
Allow Cards to Trap Int19   [No]
Memory Hole                 [Disabled]

                                        ←→   Select Screen
                                        ↑↓   Select Item
                                        +-   Change Option
                                        F1   General Help
                                        F10  Save and Exit
                                        ESC  Exit

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```

Chipset Setup Screen

When you display the Chipset Setup screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The values on the Chipset Setup screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

CHIPSET SETUP OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Chipset Setup. Once values have been defined, they display each time Chipset Setup is run.

NOTE: Do *not* change the values for the options on this screen unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

Video or Adapter ROM Shadow

ROM shadow is a technique in which BIOS code is copied from slower ROM to faster RAM. The BIOS is then executed from the RAM.

Each option allows for a segment of 16KB to be shadowed from ROM to RAM. If one of these options is enabled and there is BIOS code present in that particular segment, the BIOS is shadowed. Video BIOS shadowing may be done in two 16KB segments at C000H and C400H. Enabling shadowing can speed up the operation of a machine because RAM can be accessed more rapidly than ROM and the data bus is wider to RAM. The default setting for the video BIOS segments is **Cached**.

Other 16KB ROM segments may be shadowed in the memory area from C800H to E000H, depending upon preferences and system requirements. The ROM area that is not used by ISA adapter cards is allocated to PCI adapter cards.

The Setup screen displays the system option:

XXXX, 16k Shadow [Cached]

where XXXX is the base address of the segment of memory to be shadowed.

Three options are available:

- Select **Disabled** if you do not want to copy the specified ROM area to RAM. The contents of the video ROM cannot be read from or written to cache memory.
- Select **Enabled** to write the contents of the specified ROM area to the same address in system memory (RAM) for faster execution.
- Select **Cached** to write the contents of the specified ROM area to the same address in system memory (RAM), if an adapter ROM is using the ROM area. This also indicates that the contents of the RAM area can be read from and written to cache memory.

Memory Scrubbing

The Setup screen displays the system option:

Memory Scrubbing [Disabled]

Available options are:

Disabled
Enabled

Memory Timing Control

This option specifies whether memory timings will be selected by the user or assigned by AMIBIOS.

The Setup screen displays the system option:

Memory Timing Control [Auto]

Two options are available:

- Select **Auto** to have AMIBIOS program memory timings from Serial Presence Detect (SPD) data on the DIMM module(s).
- Select **Manual** if you want to select appropriate timings manually.

If you select **Manual**, the following options and their default values are added to the screen:

```
Act to Deact                    [5 Clks]
Act to Read/Write               [3 Clks]
RAS Precharge Time              [3 Clks]
RAS Cycle Time                  [8 Clks]
Write to Deact                  [2 Clks]
SDRAM CAS Latency               [CAS Latency 3]
```

Act to Deact

If the **Memory Timing Control** option described above is set to **Auto**, this option is not available.

The Setup screen displays the system option:

Act to Deact [5 Clks]

Available options are:

6 Clks
5 Clks

Act to Read/Write

If the **Memory Timing Control** option described above is set to **Auto**, this option is not available.

The Setup screen displays the system option:

Act to Read/Write [3 Clks]

Available options are:

3 Clks
2 Clks

RAS Precharge Time

If the **Memory Timing Control** option described above is set to **Auto**, this option is not available.

The Setup screen displays the system option:

RAS Precharge Time [3 Clks]

Available options are:

3 Clks
2 Clks

RAS Cycle Time

If the **Memory Timing Control** option described above is set to **Auto**, this option is not available.

The Setup screen displays the system option:

RAS Cycle Time [8 Clks]

Available options are:

10 Clks
9 Clks
8 Clks
7 Clks

Write to Deact

If the **Memory Timing Control** option described above is set to **Auto**, this option is not available.

The Setup screen displays the system option:

Write to Deact [2 Clks]

Available options are:

2 Clks
1 Clk

SDRAM CAS Latency

If the **Memory Timing Control** option described above is set to **Auto**, this option is not available.

The Setup screen displays the system option:

SDRAM CAS Latency [CAS Latency 3]

Available options are:

CAS Latency 3
CAS Latency 2

ISA IO Cycle Delay

The Setup screen displays the system option:

ISA IO Cycle Delay [FULL Delay]

Available options are:

FULL Delay
1.5 BCLK
2.5 BCLK
3.5 BCLK

Allow Card to Trap Int19

The Setup screen displays the system option:

Allow Card to Trap Int19 [No]

Available options are:

No
Yes

Memory Hole

This option may be used to specify an area in memory which cannot be addressed on the ISA Bus.

The Setup screen displays the system option:

Memory Hole [Disabled]

Available options are:

Disabled
15MB-16MB

Saving and Exiting

When you have made all desired changes to **Chipset Setup**, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

Chapter 6 PCI Plug and Play Setup

PCI PLUG AND PLAY SETUP

When you select **PCIPnP** from the BIOS Setup Utility Main Menu, the following Setup screen displays:

```
                              BIOS SETUP UTILITY
Main    Advanced    Chipset  |PCIPnP|   Boot   Security   Exit

OnBoard LAN1                    [Enabled]
OnBoard LAN2                    [Enabled]
OnBoard VGA                     [Enabled]
OnBoard SCSI                    [Enabled]

Plug & Play O/S                 [No]
Reset Config Data               [No]
PCI Latency Timer               [64]
Allocate IRQ to PCI VGA         [Yes]
Palette Snooping                [Disabled]
PCI IDE BusMaster               [Disabled]
OffBoard PCI/ISA IDE Card       [Auto]

USB Function                    [Enabled]
Legacy USB Support              [Auto]

IRQ3                            [Available]
IRQ4                            [Available]
IRQ5                            [Available]
IRQ7                            [Available]
IRQ9                            [Available]
IRQ10                           [Available]
IRQ11                           [Available]
IRQ14                           [Available]
IRQ15                           [Available]

DMA Channel 0                   [Available]
DMA Channel 1                   [Available]
DMA Channel 3                   [Available]
DMA Channel 5                   [Available]
DMA Channel 6                   [Available]
DMA Channel 7                   [Available]

Reserved Memory Size            [Disabled]
Reserved Memory Address         [C8000]

                                ←→   Select Screen
                                ↑↓   Select Item
                                +-   Change Option
                                F1   General Help
                                F10  Save and Exit
                                ESC  Exit

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```

PCIPnP Setup Screen

When you display the PCIPnP Setup screen, the format is similar to the sample shown above, except the screen does not display all of the options at one time. If you need to change other options, use the down arrow key to locate the appropriate option. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The values on the PCIPnP Setup screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

PCIPnP Setup Options

The descriptions for the system options listed below show the values as they appear if you have not yet run PCIPnP Setup. Once values have been defined, they display each time PCIPnP Setup is run.

NOTE: Do *not* change the values for any PCIPnP Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

OnBoard LAN1

This option indicates whether or not the first on-board Ethernet controller is to be used.

The Setup screen displays the system option:

OnBoard LAN1 [Enabled]

Available options are:

Disabled
Enabled

OnBoard LAN2

This option indicates whether or not the second on-board Ethernet controller is to be used.

The Setup screen displays the system option:

OnBoard LAN2 [Enabled]

Available options are:

Disabled
Enabled

OnBoard VGA

This option specifies whether or not the on-board video controller is to be used.

The Setup screen displays the system option:

OnBoard VGA [Enabled]

Available options are:

Disabled
Enabled

OnBoard SCSI

This option specifies whether or not the on-board SCSI controller is to be used.

The Setup screen displays the system option:

OnBoard SCSI [Enabled]

Available options are:

Disabled
Enabled

Plug & Play O/S

This option indicates whether or not the operating system installed in the computer is Plug and Play-aware. AMIBIOS only detects and enables PnP ISA adapter cards which are required for system boot. An operating system which is PnP-aware detects and enables all other PnP-aware adapter cards. Set this option to **No** if the operating system (such as DOS, OS/2, Windows 3.x) does *not* use PnP.

NOTE: You *must* set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

The Setup screen displays the system option:

Plug & Play O/S [No]

Two options are available:

- Select **No** to allow AMIBIOS to configure the devices in the system.
- Select **Yes** if your system has a Plug and Play operating system and you want to allow the operating system to configure all Plug and Play (PnP) devices which are not required for bootup.

Reset Config Data

This option specifies whether the PCI/PnP configuration data which is stored in Flash will be cleared the next time the system is booted.

The Setup screen displays the system option:

Reset Config Data [No]

Available options are:

Yes
No

PCI Latency Timer

This option specifies the latency of all PCI devices on the PCI Local Bus. The settings are in units equal to PCI clocks.

The Setup screen displays the system option:

PCI Latency Timer [64]

Available options are:

32	160
64	192
96	224
128	248

Allocate IRQ to PCI VGA

This option allows you to assign an IRQ to a PCI VGA card if the card requests an IRQ.

The Setup screen displays the system option:

Allocate IRQ to PCI VGA [Yes]

Available options are:

Yes
No

Palette Snooping

This option, when set to **Enabled**, indicates to the PCI devices that an ISA graphics device is installed in the system so the card will function correctly.

The Setup screen displays the system option:

Palette Snooping [Disabled]

Available options are:

Disabled
Enabled

PCI IDE BusMaster

This option specifies whether the IDE controller on the PCI Local Bus has bus mastering capability for reading and writing to IDE drives. The IDE drive(s) must support PCI bus mastering.

The Setup screen displays the system option:

PCI IDE BusMaster [Disabled]

Available options are:

Disabled
Enabled

OffBoard PCI/ISA IDE Card

This option specifies the PCI expansion slot on the SBC where the off-board PCI IDE controller is installed, if any.

The Setup screen displays the system option:

OffBoard PCI/ISA IDE Card [Auto]

Available options are:

Auto
PCI Slot1
PCI Slot2
PCI Slot3
PCI Slot4
PCI Slot5
PCI Slot6

If you select any value other than **Auto**, the following options and their default values are added to the screen:

```
OffBoard PCI IDE Primary IRQ   [Disabled]
OffBoard PCI IDE Secondary     [Disabled]
```

OffBoard PCI IDE Primary IRQ/OffBoard PCI IDE Secondary

These options specify the PCI interrupts used by the primary and secondary IDE channels on the off-board PCI IDE controller. You may use the **INTA**, **INTB**, **INTC** and **INTD** options to assign IRQs to the Int Pin used by the specified channel.

If the **OffBoard PCI/ISA IDE Card** option is set to **Auto**, these options are not available.

The Setup screen displays the system options:

OffBoard PCI IDE Primary IRQ [Disabled]
OffBoard PCI IDE Secondary [Disabled]

Available options are:

Disabled
INTA
INTB
INTC
INTD
Hardwired

USB Function

This option allows you to enable the Universal Serial Bus (USB).

The Setup screen displays the system option:

USB Function [Enabled]

Available options are:

Disabled
Enabled

Legacy USB Support

This option allows you to enable support for older USB devices.

The Setup screen displays the system option:

Legacy USB Support [Auto]

Available options are:

Disabled
Enabled
Auto

IRQ3/IRQ4/IRQ5/IRQ7/IRQ9/IRQ10/IRQ11/IRQ14/IRQ15

These options indicate whether the specified interrupt request (IRQ) is available for use by the system for PCI/Plug and Play devices or is reserved for use by legacy devices. This allows you to specify IRQs for use by legacy ISA adapter cards.

The IRQ setup options indicate whether AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices.

The Setup screen displays the system option:

IRQ# **[Available]**

where # is the number of the interrupt request (IRQ)

Two options are available:

- Select **Available** to make the specified IRQ available for use by PCI/PnP devices.
- Select **Reserved** to reserve the specified IRQ for use by legacy ISA devices.

DMA Channels 0, 1, 3, 5, 6 and 7

These options indicate whether the specified DMA channel is available for use by the system for PCI/Plug and Play devices or is reserved for use by legacy ISA devices.

The Setup screen displays the system option:

DMA Channel # **[Available]**

where # is the DMA Channel number

Two options are available:

- **Available** indicates that the specified DMA channel is available for use by PCI/PnP devices.
- **Reserved** indicates the specified DMA channel is reserved for use by legacy ISA devices.

Reserved Memory Size

This option specifies the size of the memory area reserved for legacy ISA adapter cards.

If this option is set to **Disabled**, the **Reserved Memory Address** option is not available.

The Setup screen displays the system option:

Reserved Memory Size **[Disabled]**

Available options are:

Disabled
16k
32k
64k

Reserved Memory Address

This option specifies the beginning address (in hexadecimal) of the ROM memory area reserved for use by legacy ISA adapter cards.

If the **Reserved Memory Size** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Reserved Memory Address [C8000]

Available options are:

C0000	D0000
C4000	D4000
C8000	D8000
CC000	DC000

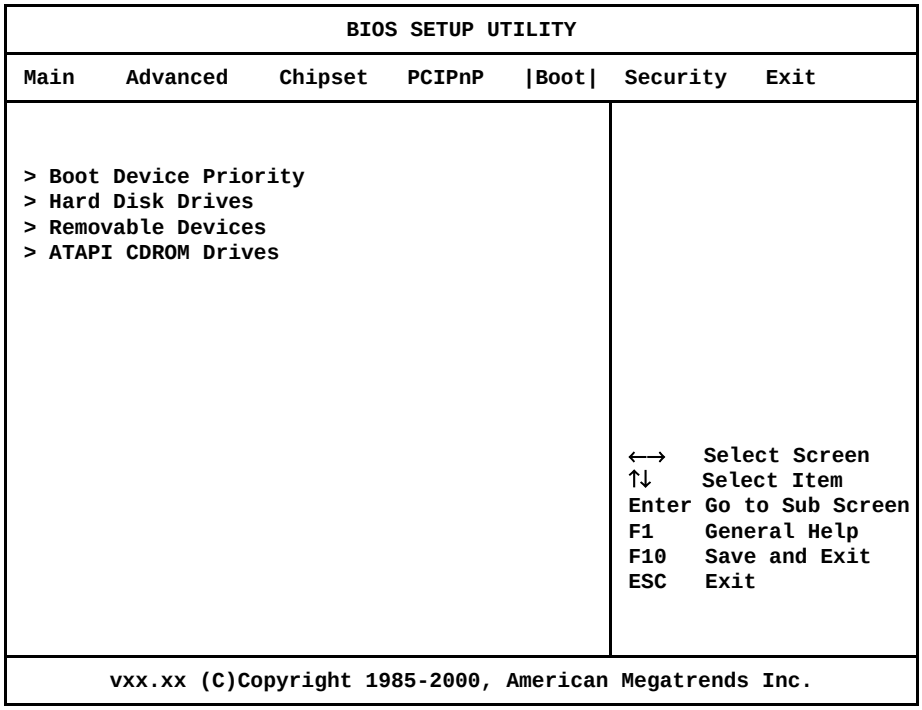
Saving and Exiting

When you have made all desired changes to PCIPnP Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

Chapter 7 Boot Setup

BOOT SETUP

When you select **Boot** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Boot Setup Screen

When you display the Boot Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Boot Setup options. Highlight the option you wish to change and press **<Enter>** to go to the appropriate subscreen.

NOTE: If no device is found for one of the device types, the line item for that device type does not display.

BOOT SETUP OPTIONS

The Boot Setup options allow you to specify the boot sequence of bootable devices in your system.

Boot Device Priority

The options on the **Boot Device Priority** subscreen specify the order in which AMIBIOS attempts to boot devices available in the system. It allows you to select the type of drive which will be booted first, second, third, etc. If there are multiple drives of a particular type, you may specify the order in which each drive of that type will be selected by using the other options on the Boot Setup Menu.

Hard Disk Drives

The **Hard Disk Drives** subscreen specifies the boot sequence of the hard drives available in the system.

Removable Devices

The **Removable Devices** subscreen specifies the boot sequence of the removable devices available in the system.

ATAPI CDROM Drives

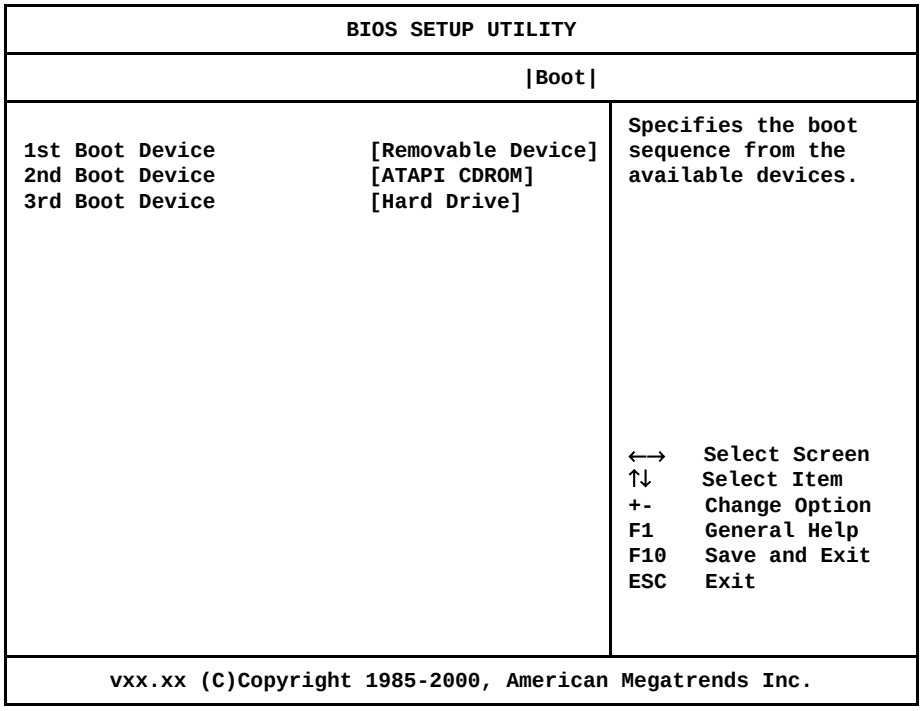
The **ATAPI CDROM Drives** subscreen specifies the boot sequence of the ATAPI CDROM devices available in the system.

Saving and Exiting

When you have made all desired changes to **Boot Setup**, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

BOOT DEVICE PRIORITY

When you select **Boot Device Priority** from the Boot Setup Menu, the following Setup screen displays:



Boot Device Priority Screen

When you display the Boot Device Priority screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The number of line items on this screen may vary depending on the number of bootable devices available on your system.

BOOT DEVICE PRIORITY OPTIONS

1st Boot Device/2nd Boot Device/3rd Boot Device

This option specifies the device type of each boot drive from which AMIBIOS attempts to boot after the POST routines complete. Available options for each boot device line item are determined by the types of bootable devices available on your system.

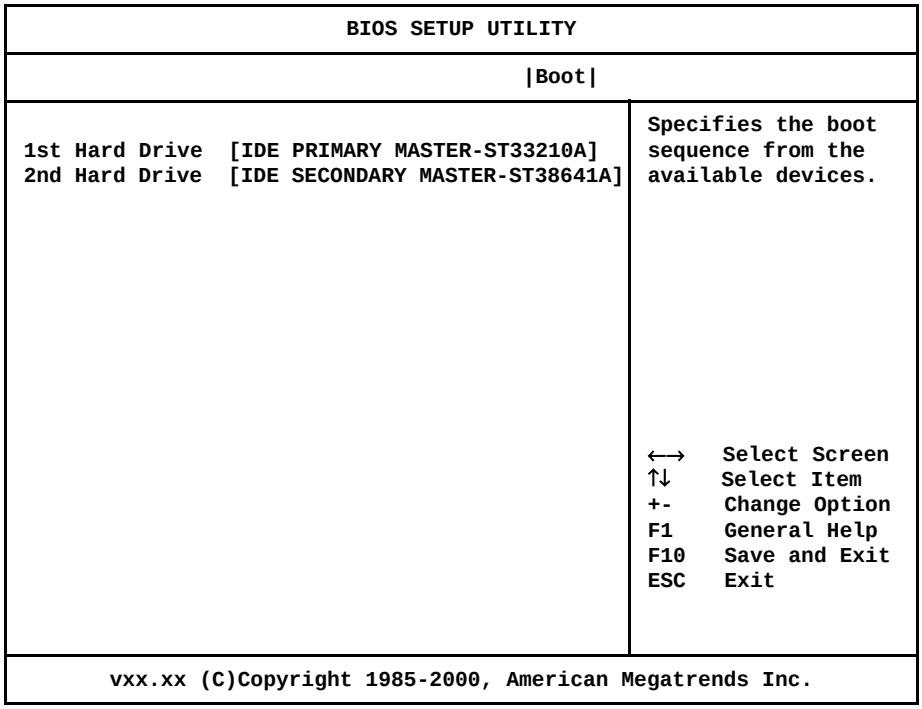
The Setup screen displays the system option(s):

1st Boot Device	**[Removable Device]**
2nd Boot Device	**[ATAPI CDROM]**
3rd Boot Device	**[Hard Drive]**

Available options are:

Removable Device
ATAPI CDROM
Hard Drive

HARD DISK DRIVES When you select **Hard Disk Drives** from the Boot Setup Menu, the following Setup screen displays:



Hard Disk Drives Screen

When you display the Hard Disk Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: This screen is available only if there is at least one hard disk drive on your system. The number of line items is determined by the number of hard disk drives available.

HARD DISK DRIVES OPTIONS The SBC supports up to four hard disk drives through a primary and secondary controller in a master/slave configuration.

When the system boots up, it searches for all hard drives and displays the description of each hard drive it has detected and the controller on which it is found.

1st Hard Drive/2nd Hard Drive

If you have more than one hard disk drive, you may change the order in which the system will attempt to boot the available hard drives by changing these line items.

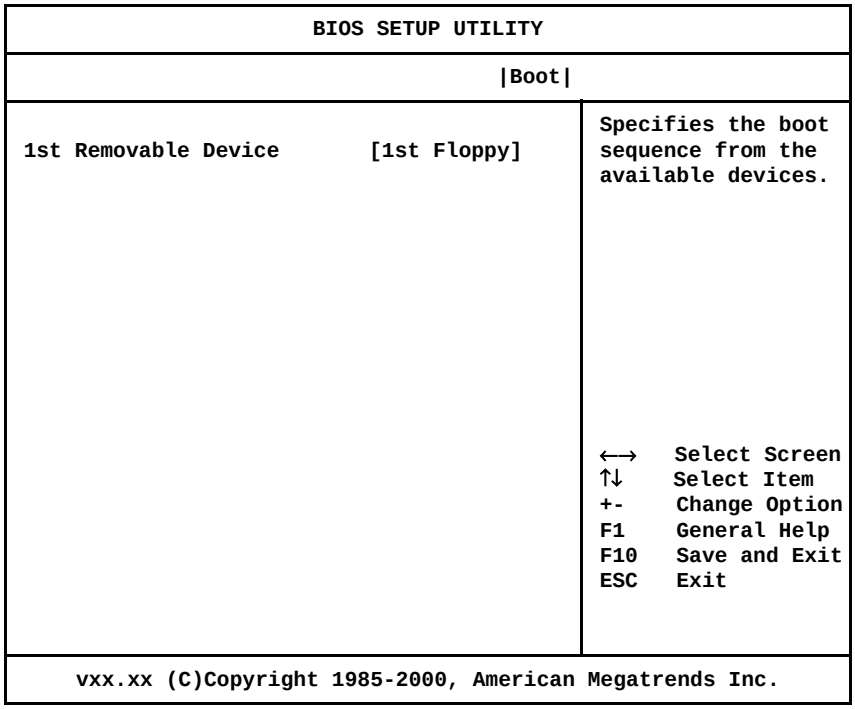
The Setup screen displays the system options:

1st Hard Drive	[IDE PRIMARY MASTER - xxxxxxxx]
2nd Hard Drive	[IDE SECONDARY MASTER - xxxxxxxx]

where xxxxxxxx is the description of the hard drive

REMOVABLE DEVICES

When you select **Removable Devices** from the Boot Setup Menu, the following Setup screen displays:



Removable Devices Screen

When you display the Removable Devices screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: This screen is available only if there is at least one removable device on your system. The number of line items is determined by the number of removable devices available.

REMOVABLE DEVICES OPTIONS

When the system boots up, it searches for all removable devices and displays the description of each device it has detected.

1st Removable Device

If you have more than one removable device, you may change the order in which the system will attempt to boot the available devices by changing these line items.

The Setup screen displays the system option:

1st Removable Device [1st Floppy]

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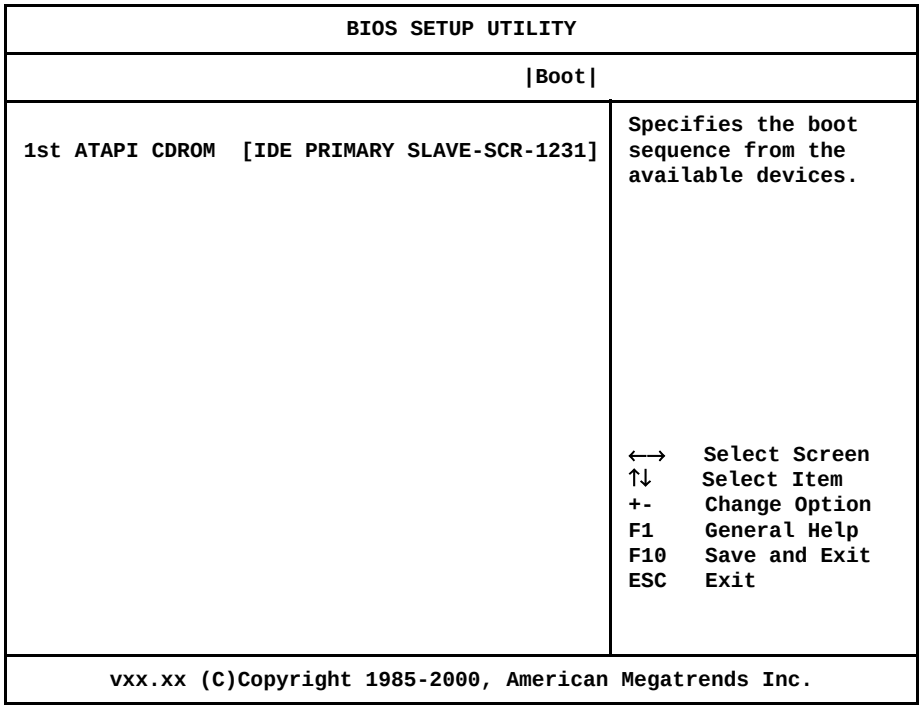
ATAPI CDROM DRIVES

When you select **ATAPI CDROM Drives** from the Boot Setup Menu, the following Setup screen displays:



ATAPI CDROM Drives Screen

When you display the ATAPI CDROM Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: This screen is available only if there is at least one ATAPI CDROM drive on your system. The number of line items is determined by the number of ATAPI CDROM drives available.

ATAPI CDROM DRIVES OPTIONS

When the system boots up, it searches for all ATAPI CDROM drives and displays the description of each ATAPI CDROM drive it has detected and the controller on which it is found.

1st ATAPI CDROM

If you have more than one ATAPI CDROM drive, you may change the order in which the system will attempt to boot the available drives by changing these line items.

The Setup screen displays the system option:

1st ATAPI CDROM [IDE PRIMARY SLAVE - xxxxxxxx]

where xxxxxxxx is the description of the ATAPI CDROM drive

Appendix A BIOS Messages

BIOS BEEP CODES

Errors may occur during the POST (Power-On Self Test) routines which are performed each time the system is powered on.

Non-fatal errors are those which, in most cases, allow the system to continue the bootup process. The error message normally appears on the screen. See *BIOS Error Messages* later in this appendix for descriptions of these messages.

Fatal errors are those which will not allow the system to continue the bootup procedure.

These fatal errors are usually communicated through a series of audible beeps. Each error message has its own specific beep code, defined by the number of beeps following the error detection. The following table lists the errors which are communicated audibly.

All errors listed, *with the exception of #8*, are fatal errors.

Beep Count	Message	Description
1	Refresh Failure	The memory refresh circuitry of the processor board is faulty.
2	Parity Error	A parity error was detected in the base memory (the first block of 64KB) of the system.
3	Base 64KB Memory Failure	A memory failure occurred within the first 64KB of memory.
4	Timer Not Operational	A memory failure occurred within the first 64KB of memory, or Timer #1 on the processor board has failed to function properly.
5	Processor Error	The CPU (Central Processing Unit) on the processor board has generated an error.
6	8042 - Gate A20 Failure	The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in protected mode. This error message means that the BIOS is not able to switch the CPU into protected mode.
7	Processor Exception Interrupt Error	The CPU on the processor board has generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. **NOTE:** This is *not* a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in the BIOS.

BIOS BEEP CODES (CONTINUED)

Beep Count	Message	Description
10	CMOS Shutdown Register Read/Write Error	The shutdown register for the CMOS RAM has failed.
11	Cache Memory Bad; Do Not Enable Cache	The cache memory test failed. Cache memory is disabled. *Do not press <Ctrl><Alt><Shift><+> to enable cache memory.*

BIOS ERROR MESSAGES

If a non-fatal error occurs during the POST routines performed each time the system is powered on, the error message will appear on the screen in the following format:

ERROR Message Line 1
ERROR Message Line 2
Press F1 to Resume

Note the error message and press the **<F1>** key to continue with the bootup procedure.

NOTE: If the **Wait for 'F1' If Any Error** option in the Advanced Setup portion of the BIOS Setup Program has been set to **Disabled**, the "Press F1 to Resume" prompt will not appear on the last line. The bootup procedure will continue without waiting for operator response.

For most of the error messages, there is no ERROR Message Line 2. Generally, for those messages containing an ERROR Message Line 2, the text will be "RUN SETUP UTILITY." Pressing the **<F1>** key will invoke the BIOS Setup Utility.

A description of each error message appears below. The errors are listed in alphabetical order, not in the order in which they may occur.

Message	Description
8042 Gate-A20 Error	The gate-A20 portion of the keyboard controller (8042) has failed to operate correctly. Replace the 8042 chip.
Address Line Short!	An error has occurred in the address decoding circuitry of the processor board.
C: Drive Error	The BIOS is not receiving any response from hard disk drive C:. Check Standard Setup using the BIOS Setup Utility to see if the correct hard disk drive has been selected.
C: Drive Failure	The BIOS cannot get *any* response from hard disk drive C:. It may be necessary to replace the hard disk.
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective.

BIOS ERROR MESSAGES (CONTINUED)

Message	Description
CH-2 Timer Error	Most AT standard system boards include two timers. An error with Timer #1 is a fatal error, explained in *BIOS Beep Codes* earlier in this appendix. If an error occurs with Timer #2, this error message appears.
CMOS Battery State Low	There is a battery in the system which is used for storing the CMOS values. This battery appears to be low in power and needs to be replaced.
CMOS Checksum Failure	After the CMOS values are saved, a checksum value is generated to provide for error checking. If the previous value is different from the value currently read, this error message appears. To correct the error, run the BIOS Setup Utility.
CMOS Display Type Mismatch	The type of video stored in CMOS does not match the type detected by the BIOS. Run the BIOS Setup Utility to correct the error.
CMOS Memory Size Mismatch	If the BIOS finds the amount of memory on the system board to be different from the amount stored in CMOS, this error message is generated. Run the BIOS Setup Utility to correct the error.
CMOS System Options Not Set	The values stored in the CMOS are either corrupt or nonexistent. Run the BIOS Setup Utility to correct the error.
CMOS Time & Date Not Set	Use Standard Setup in the BIOS Setup Utility to set the date and time of the CMOS.
D: Drive Error	The BIOS is not receiving any response from hard disk drive D:. Check Standard Setup using the BIOS Setup Utility to see if the correct hard disk drive has been selected.
D: Drive Failure	The BIOS cannot get *any* response from hard disk drive C:. It may be necessary to replace the hard disk.
Diskette Boot Failure	The disk used to boot up in floppy drive A: is corrupt, which means it cannot be used to boot up the system. Use another boot disk and follow the instructions on the screen.
Display Switch Not Proper	Some systems require that a video switch on the processor be set to either color or monochrome, depending upon the type of video being used. To correct this situation, set the switch properly after the system is powered off.
DMA Error	An error has occurred in the DMA controller on the processor board.
DMA #1 Error	An error has occurred in the first DMA channel on the processor board.
DMA #2 Error	An error has occurred in the second DMA channel on the processor board.
FDD Controller Failure	The BIOS is not able to communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered off.

BIOS ERROR MESSAGES (CONTINUED)

Message	Description
HDD Controller Failure	The BIOS is not able to communicate with the hard disk drive controller. Check all appropriate connections after the system is powered off.
INTR #1 Error	Interrupt channel #1 has failed the POST routine.
INTR #2 Error	Interrupt channel #2 has failed the POST routine.
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but it *cannot* boot up the system with it. Use another boot disk and follow the instructions on the screen.
KB/Interface Error	The BIOS has found an error with the keyboard connector on the processor board.
Keyboard Error	The BIOS has encountered a timing problem with the keyboard. The Keyboard option in the Standard Setup portion of the BIOS Setup Utility may be set to **Not Installed**, which will cause the BIOS to skip the keyboard POST routines.
Keyboard Is Locked... Unlock It	The keyboard lock on the system is engaged. It must be unlocked to continue the bootup procedure.
No ROM BASIC	This error occurs when a proper bootable sector cannot be found on either floppy disk drive A: or hard disk drive C:. The BIOS will try at this point to run ROM Basic, and the error message is generated when the BIOS does not find it.
Off Board Parity Error	The BIOS has encountered a parity error in memory installed on an adapter card in an I/O (Bus) expansion slot. The message appears as follows: OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX) where XXXX is the address (in hexadecimal) at which the error has occurred. "Off Board" means that it is part of the memory installed via an expansion card in an I/O (Bus) slot, as opposed to memory attached directly to the processor board.
On Board Parity Error	The BIOS has encountered a parity error in memory installed on the processor board. The message appears as follows: ON BOARD PARITY ERROR ADDR (HEX) = (XXXX) where XXXX is the address (in hexadecimal) at which the error has occurred. "On Board" means that it is part of the memory directly attached to the processor board, as opposed to memory installed via an expansion card in an I/O (Bus) slot.
Parity Error ????	The BIOS has encountered a parity error with some memory in the system, but it is not able to determine the address of the error.

ISA BIOS NMI HANDLER MESSAGES

Message	Description
Memory Parity Error	Memory failed. The message appears as follows: MEMORY PARITY ERROR AT XXXXX where XXXXX is the address (in hexadecimal) at which the error has occurred. If the memory location cannot be determined, the message is “Memory Parity Error ????”
I/O Card Parity Error	An expansion card failed. The message appears as follows: I/O PARITY ERROR AT XXXXX where XXXXX is the address (in hexadecimal) at which the error has occurred. If the address cannot be determined, the message is “I/O Card Parity Error ????”
DMA Bus Time-Out	A device has driven the bus signal for more than 7.8 micro-seconds.

BOOTBLOCK INITIALIZATION CODE CHECKPOINTS

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the Bootblock initialization portion of the BIOS:

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum. Execute OEM memory patch.
D2	Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Verify that flat mode is enabled.
D4	Test base 512K memory. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See the *Bootblock Recovery Code Checkpoints* section of this appendix for more information.
D7	Hard reset is simulated by programming the keyboard controller. Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Runtime is moved to F000 shadow. E000 shadow is initialized with E000 ROM code. Restore CPUID value back into register. Give control to F000 shadow at F000:FFF0h. Control flows to checkpoint 03. See the *POST Code Checkpoints* section of this appendix for more information.

BOOTBLOCK RECOVERY CODE CHECKPOINTS

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Check-point	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
E9 or EA	Determine information about root directory of recovery media.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

POST CODE CHECKPOINTS

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Check-point	Description
03	Disable video for EGA and monochrome devices. Determine whether this boot is a soft reset or power-on. Set BIOS stack. Go to flat mode. Initialize base 640KB of memory. Fill in POST, runtime and INT13 interface information in runtime module header.
05	Stop USB host controller. Disable all cache.
06	Uncompress POST module into memory. Fill in POST interface information in runtime module header. Fill in POST, runtime and INT13 interface information in POST module header. Give control to POST module. Uncompress various modules (debug, DIM and INT10) and place them in their appropriate places.
08	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Clear CMOS pending interrupt. Initialize status register A.
07	Initialize data area used by BIOS Update (CPU microcode) functions. Do early CPU initializations including initialization of CPU, SMI info and CPU name display buffers, initialization of BSP and AP processors. and enabling of L1 cache. Verify that flat mode is enabled. Initialize RT_CMOS_BYTE. Initialize INT13 interrupt service routines to just return.
0B	Perform any chipset or OEM initialization before keyboard BAT test is done.
0C	Issue the BAT command to the keyboard controller.
0E	Perform any chipset or OEM initialization after keyboard BAT test is done.
0F	Program the keyboard controller command byte.
11	Check for INS, END and DEL key. Get POST flags for clearing CMOS, clearing passwords and executing setup. Clear CMOS if POST flag is set.
12	Initialize CMOS and checksum with default values if END is pressed, “initialize CMOS in every boot” flag is set, or OEM method flag is set. Disable DMA and interrupt controllers. Disable video for EGA and monochrome devices.
13	Check for DEL or alternate key to enter setup. The DEL key is also checked in the majority of the checkpoints from checkpoint 13 to checkpoint 40. Initialize the chipset.
14	Perform 8259 timer test on channel 2.
19	Test memory refresh.
1A	Continue testing memory refresh. Clear parity status. Parity status is cleared many times in checkpoints following 1A.
23	Read PC switch settings. Initialize Green KBC settings.

POST CODE CHECKPOINTS (CONTINUED)

Check-point	Description
24	Perform any chipset or OEM initialization before the interrupt vector table is initialized. Determine the processor board.
25	Initialize interrupt vector table. Clear passwords if POST flag is set.
27	Enable USB function and set USB clock if configurable. Uncompress GPC module. Initialize SMI handler for AP processors. Initialize GPC for USB support. Perform any chipset or OEM initialization before the memory test is done.
28	Set monochrome and color mode video settings.
29	Call debugger hook.
2A	Initialize different buses through DIM module. See the *DIM Code Checkpoints* section of this appendix for more information.
2B	Call hook that is available to initialize a video ROM if DIM code has not already initialized video.
2C	Search for and give control to the video ROM if not already done by DIM code.
2D	Uncompress the ADM module and initialize it. Initialize small and silent logo data areas including uncompressing of logo modules. Detect the presence of a PS/2 mouse. Establish link for console redirection. Perform any chipset or OEM initialization after video has been initialized.
2E	Detect type of video present.
2F	Execute display memory read/write test.
30	Perform refresh retrace tests.
31	Execute alternate display memory read/write test.
32	Perform alternate refresh retrace tests.
34	Set display mode.
37	Initialize ADM for display. Initialize silent boot. Display sign-on message. Display any chipset or OEM message strings after sign-on message has been displayed.
38	Initialize different buses through DIM module. See the *DIM Code Checkpoints* section of this appendix for more information. Verify that flat mode is enabled. Detect the presence of a USB mouse. Display NVRAM message. Initialize ATA channel details in runtime segment. Rest hard disk controller. Uncompress HHF module.
39	Display any errors reported by DIM. See the *DIM Code Checkpoints* section of this appendix for more information. Display USB devices found. Display any chipset or OEM message strings before memory count begins.
3A	Display message to press a key to enter setup. Display entering setup message if DEL key has been pressed.

POST CODE CHECKPOINTS (CONTINUED)

Check-point	Description
40	Check for DEL or ESC keys to limit memory test. The DEL and ESC keys are also checked in the majority of the checkpoints from checkpoint 40 to checkpoint 59. Initialize the global data areas with variables used during memory test, including quick boot, tick sound and above 1MB memory test.
43	Enable interrupts.
45	Determine number of 64KB blocks above and below 1MB.
4B	Check for soft reset.
4C	Clear all memory and do not perform memory test if soft reset has occurred.
4E	Display initial memory size count as 128KB.
4F	Check to see if quick boot is enabled. Perform pattern test on memory below 1MB. Display memory size count as memory test continues.
50	Determine whether to count and display extra 384KB of memory from A0000 to FFFFF. Display and clear total memory present if memory test has been bypassed. Check global data variable to determine whether to test memory above 1MB.
51	Perform pattern test on extended memory. Display memory size count as memory test continues.
52	Save amount of base and extended memory into CMOS.
53	Clear parity status.
54	Disable parity and NMI. Initialize CMOS memory locations and checksum if “initialize CMOS in every boot” flag is set.
57	Perform any chipset or OEM initialization after memory test has been done. This may include programming holes in memory. Initialize the last extended memory address for PMM.
58	Display messages including “Wait” string.
59	Disable DMA controller. Determine if DMA controller should be tested or if DMA registers should be preserved. Perform port pattern test on DMA registers.
60	Determine if DMA controller should be tested or if DMA registers should be preserved. Perform port pattern test on DMA 1 registers.
62	Perform port pattern test on DMA 2 registers.
65	Initialize DMA units 1 and 2.
66	Initialize interrupt controller.
67	Initialize and set master and slave interrupt controller masks.
7F	Reset interrupt vector used for silent boot. Call DIM code to enable extended NMI for EISA sources.

POST CODE CHECKPOINTS (CONTINUED)

Check-point	Description
80	Program PS/2 mouse as edge or level interrupt.
81	Test and initialize the keyboard, including checking for a stuck key and locked keyboard and enabling necessary interrupts.
83	Disable parity and NMI. Set interrupt vector used for silent boot. Call optional OEM patch. Update CMOS memory locations and checksum if memory size mismatch error has occurred.
84	Set error bit if memory size mismatch has occurred. Set memory expansion bit in CMOS correctly. Allocate EBDA. Uncompress INT13 module into memory. Give control to INT13 initialization code. Initialize ATA/ATAPI data area. Detect presence of a floppy. Call DIM module to scan and initialize BBS option ROMs. See *DIM Code Checkpoints* section of this appendix for more information. Test and initialize the keyboard, including checking for a stuck key and locked keyboard and enabling necessary interrupts. Check for presence of keyboard and video in order to set error bits. Identify attached ATAPI devices. Initialize POST error information for event logging.
85	Display any error messages. Wait for F1 and F2 keystrokes. Determine whether setup can be executed according to POST flag. Check password 3 times and load CMOS and GPNV default values if F2 was pressed. Determine if user wants and is permitted to enter setup and force display back to BIOS. Set up printer values to allow Print Screen to work in setup. Reset the mouse if a USB mouse is present.
86	Perform any chipset or OEM initialization before CMOS setup is executed.
87	Execute CMOS setup program. Display “Wait” message.
88	Establish link for console redirection. Perform any chipset or OEM initialization after CMOS setup has executed.
89	Reboot system if keyboard is locked. Restore previous POST display mode. Display “Wait” message.
8B	Deallocate all memory used for HHF. Initialize the boot device order and associated variables.
8C	Perform any chipset or OEM initialization after CMOS setup even if not executed. Several items initialized are the INT15 E820 table, chipset and I/O setup parameters, and ACPI tables.
8D	Call optional OEM patch. Initialize printer and serial time-out values.
95	Check and load unattended password. Restore display from silent mode to BIOS. Initialize the boot device order and associated variables.
8E	Uncompress INT13 module into memory. Prepare the INT13 module and associated variables, including virus protection setting, for FDD, ATA and ATAPI devices.
93	Modify variables according to presence of SCSI drives. Check if I2O device is a boot device. Give control to INT13 module. Initialize the data area used by ATA and ATAPI devices.

POST CODE CHECKPOINTS (CONTINUED)

Check-point	Description
8F	Initialize the floppy disk drive, including initializing the global data area, setting interrupt vectors and sensing drive type and setting disk state accordingly. Initialize AFD variables.
91	Initialize ATA and ATAPI devices and associated variables.
92	Initialize I2O devices and associated variables. Adjust AFD variables. Call DIM module to scan and initialize option ROMs. See *DIM Code Checkpoints* section of this appendix for more information.
96	Call hook that is available to initialize option ROMs if DIM code has not already initialized any.
97	Search for and give control to the option ROMs if not already done by DIM code.
98	Restore the original mode of the video display. Stop USB host controller. Establish link for console redirection. Restart USB host.
99	Check for valid RTC date and time. Initialize date and time to valid setting if corrupt. Detect and initialize parallel port I/O addresses.
9A	Detect and initialize serial port I/O addresses.
9B	Perform any chipset or OEM initialization before co-processor check.
9C	Initialize 80287 numeric processor.
9D	Perform any chipset or OEM initialization after co-processor check. Update equipment byte in CMOS.
A2	Initialize POST error information for event logging. Display any SMART error messages. Display any error message from the 2nd set. Wait for F1 key to resume if necessary.
A4	Call hook to perform any chipset or OEM time dependent programming.
A5	Output a single beep to the PC speaker.
A7	Call optional OEM patch. Start to prepare the final runtime image before copying it into F000 shadow.
AE	Uncompress the DMI module and give it control in order to build the DMI data structures. Move the DMI code and structures into the final runtime image.
AC	Uncompress the MP module and give it control in order to build the MP table. Move the MP table into the final runtime image.
AB	Prepare the final INT13 image. Move the INT13 code into the final runtime image.
AD	Prepare the final INT10 image. Move the INT10 code into the final runtime image in F000 or leave it in E000. Update necessary data in different modules after all the modules are put in the final runtime segment. Perform any chipset or OEM initialization before an option ROM at E000 is given control. Flush all cache. Make F000 shadow read-only.

POST CODE CHECKPOINTS (CONTINUED)

Check-point	Description
A8	Test for valid ROM at E000 and give it control. Make F000 shadow read-write.
A9	Establish link for console redirection. Perform any chipset or OEM initialization after an option ROM at E000 is given control.
AA	Clear the screen. Maximize BIOS display window. Display the BIOS configuration screen that includes information on the type of processor, cache, floppy and info on many other generic system components. Display any chipset or OEM messages. Stop the USB host controller. Set up the USB controller according to the user setup selection. Program the typematic rate and initial NUM-LOCK setting. Check and load unattended password. Disable console redirection. Initialize the CPUs before boot, which includes the programming of the MTRRs. Give pause before booting if necessary. Initialize MS IRQ routing table. Prepare language and ADM module for runtime.
B1	Perform any chipset or OEM initialization after the BIOS configuration screen is displayed and before INT19 booting occurs. Save ACPI related system context.
00	Clear any data area used by the BIOS before issuing an INT19. Issue an INT19 to start BIOS routine for booting a device.

DIM CODE CHECKPOINTS

The Device Initialization Manager module gets control at various times during BIOS POST to initialize different buses. The following table describes the main checkpoints where the DIM module is accessed:

Check-point	Description
2A	Initialize different buses and perform the following functions: Reset, Detect and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices and PnP ISA cards. It also assigns PCI Bus numbers. Function 1 initializes all static devices, which include manually configured on-board peripherals, memory and I/O decode windows in PCI-to-PCI bridges and non-compliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI or AGP video drivers.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all on-board peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.
39	Display error messages encountered during initialization of different buses. Perform function 6, which returns error flags that are used to display necessary error information.
84	Scan and initialize BBS option ROMs. Perform function 8, which builds various IPL tables according to the boot devices present in the system.
92	Scan and initialize option ROMs. Perform function 7, which gives control and shadows all present ISA, PnP ISA and PCI option ROMs.

ADDITIONAL CHECKPOINTS

While control is in the different functions, additional checkpoints are output to Port 80H as word values to identify the routines being executed.

The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two sets of information. The details of the high byte of these checkpoints are detailed in the following table:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0	Function 0. Disable all devices on the bus.
1	Function 1. Initialize static devices on the bus.
2	Function 2. Initialize output devices on the bus.
3	Function 3. Initialize input devices on the bus.
4	Function 4. Initialize IPL devices on the bus.
5	Function 5. Initialize general devices on the bus.
6	Function 6. Initialize error reporting for the bus.
7	Function 7. Initialize add-on ROMs for all buses.

The lower nibble 'Y' indicates the bus on which the different routines are being executed. 'Y' can be from 0 to 5.

0	Generic DIM (Device Initialization Manager)
1	On-board system devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

Declaration of Conformity

APPLICATION OF COUNCIL DIRECTIVE(S)

89/336/EEC

Standard(s) to which Conformity is Declared:

EN61000-6-2: 1999; EN55022: 1998, CLASS B
EN61000-3-2: 1995/A2: 1998; EN61000-3-3: 1995

Manufacturer:	TRENTON TECHNOLOGY Inc. 2350 Centennial Drive Gainesville, Georgia 30504 USA Telephone: (770) 287-3100 FAX: (770) 287-3150
Type of Equipment:	PCI CPU Board
Model Name(s):	92-005891 (Also Known As: SLE/1.4, SLE/1.26, SLE/1.13, SLE/1.0B, SLE/933, SLE/866, SLE/800EB, SLE/733, SLE/667 and SLE/600EB)

I, the undersigned, hereby declare that the specified equipment conforms to the Directive(s) and Standard(s) listed above.

Name:	Charles B. Hinson
Title:	Development Quality Assurance Manager
Date:	October 10, 2002

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