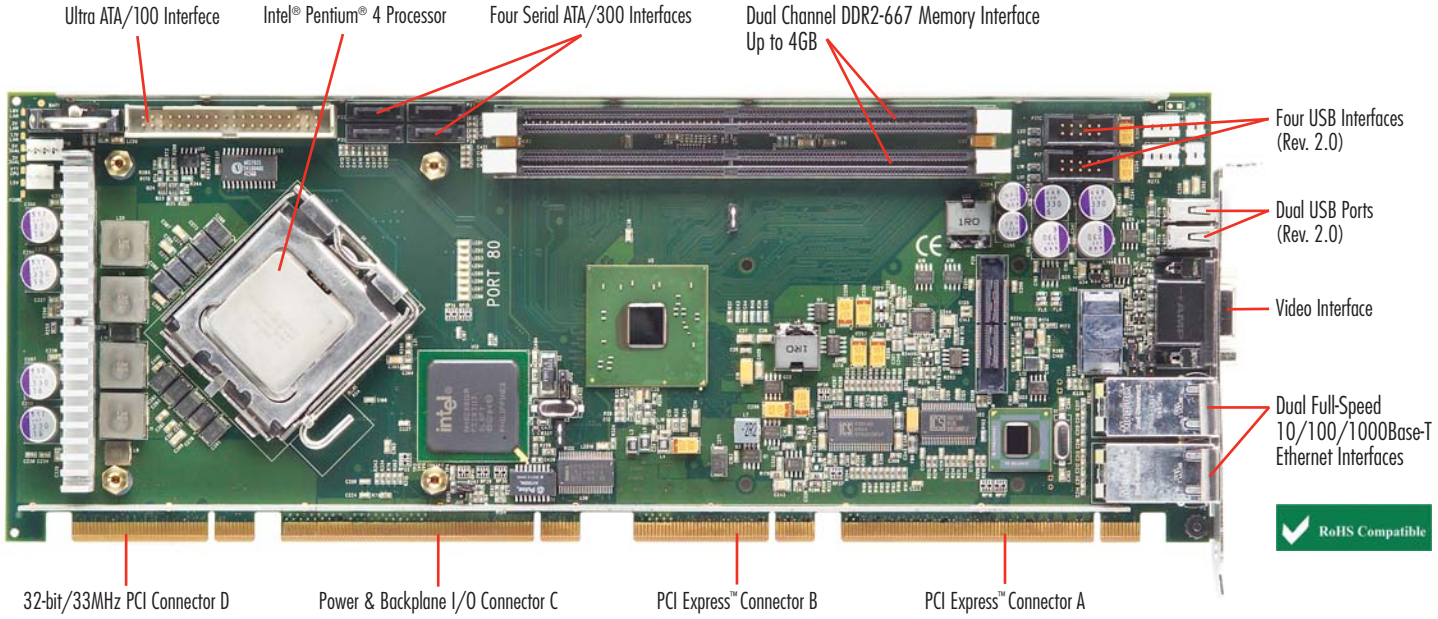
T4L

PRODUCT DATA SHEET

T4L (SHB Express™) SYSTEM HOST BOARD



Trenton's T4L is a graphics-class, PICMG® 1.3 system host board that offers flexibility, performance and value. The SHB supports x16, x4 and x1 PCI Express™ links, and a 32-bit/33MHz PCI interface to a PICMG 1.3 backplane. The T4L handles a wide range of system option cards, from the latest x16 PCI Express video cards to legacy 32-bit/33MHz PCI cards. Socket-LGA775 processor options have larger L2 cache memories and faster system bus architectures. The Intel® 945G MCH and Intel® ICH7R ICH deliver advanced T4L capabilities for demanding applications.

PROCESSOR:

Intel® Pentium® 4 Processor at 3.0GHz to 3.8GHz*
Processor Package: FC-LGA4, plugs into an LGA775 socket

**Higher speeds as available*

The Intel® processor options on the T4L support a 1066MHz, 800MHz or 533MHz system bus depending on the choice of processor. All of the processor options support both 64-bit and 32-bit applications. Intel® Extended Memory 64 Technology (Intel® EM64T) is the processor feature that allows 64-bit application support. Other processor features:

- Hyper-Threading Technology
- 1M or 2M L2 Cache

CHIPSET:

The Intel® 945G chipset combines advanced video and graphics capabilities with high-bandwidth interfaces such as a dual-channel DDR2-667, 1066MHz FSB, PCI Express x16 graphics port and PCI Express x4 and x1 links to a PICMG 1.3 backplane. An Intel® ICH7R provides eight USB 2.0 and four SATA/300 ports. The ICH7R's SATA controller supports independent DMA, Advanced Host Controller Interface (AHCI) and integrated RAID level 0, 1, 5 and 10 functionality.

PCI EXPRESS™ INTERFACES:

Trenton's T4L graphics-class system host board provides one x16 PCI Express link on the SHB's edge connectors A and B. This x16 PCIe link is designed to support PCI Express video/graphics cards on an SHB Express™ (PICMG 1.3) backplane. A x4 PCI Express link and five PCI Express reference clocks are also included on edge connectors A and B. An additional x1 PCI Express link between the T4L and backplane can be provided by Trenton's optional IOB31 I/O Expansion Module. The x4 and x1 PCI Express links are used on SHB Express backplanes to support PCI Express option cards and the bridge chips that provide PCI/PCI-X option card support. During system initialization the T4L automatically negotiates with the PCI Express cards connected to the PCI Express links in order to set up communication between the devices. The net result is that the T4L system host board supports communication to x1, x4, x8 and x16 PCI Express boards as well as PCI/PCI-X cards via PCI Express-to-PCI/PCI-X bridge chip technology. The T4L also provides a 32-bit/33MHz PCI bus interface on edge connector D.

DDR2-667 MEMORY:

The DDR2-667 interface is a dual-channel interface originating at the Memory Controller Hub, with each channel terminating at a DIMM module socket. The T4L supports system memory transfer rates of either 400, 533 or 667MHz using unbuffered, non-ECC, PC2-3200, PC2-4200 or PC2-5300 DIMMs. Maximum memory capacity is 4GB. When using a single PC2-5300 DIMM, the memory interface bandwidth is 5.4GB/s, and when using two PC2-5300 DIMMs with equal memory capacities the T4L's peak memory bandwidth increases to 10.7GB/s.

VIDEO INTERFACE:

The T4L supports three video connection options:

- Direct connection via the chipset's Intel Graphics Media Accelerator 950 with faster graphics and 3D performance
- A x16 PCI Express graphics port that provides 3.5 times more bandwidth than an AGP 8X interface
- ADD2 video and graphic cards

PCI EXPRESS™ CONFIGURATION AND BUS SPEEDS:

PCI Express - Edge Connectors A & B	- One x16 link, one x4 link - Five reference clocks
PCI Express - (on-board only)	- Two x1 links
PCI	- 32-bit/33MHz
System or FSB	- 1066MHz, 800MHz or 533MHz

SERIAL ATA/300 PORTS (FOUR):

The primary and secondary Serial ATA (SATA) ports on the T4L board support four independent SATA storage devices such as hard disks and CD-RW devices. SATA produces higher performance interfacing by providing data transfer rates up to 300MB per second on each port. The T4L's ICH7R I/O Controller hub features Intel® Matrix Storage Technology, which allows the ICH7R's SATA controller to be configured as a RAID controller supporting RAID 0, 1, 5, and 10 implementations.

ETHERNET INTERFACES:

The T4L uses an internal x1 PCI Express link to connect the I/O Controller hub to the dual-port Gigabit Ethernet controller chip. This design feature enables dual 10/100/1000Base-T Ethernet interfaces on LAN 1 and LAN2. The LAN ports have RJ-45 connectors on the I/O bracket to provide the mechanical interfaces to the Ethernet networks. The ICH7R's internal LAN Interconnect Interface (LCI) provides an additional 10/100Base-T Ethernet interface for use on PICMG® 1.3 backplanes via the SHB's edge connector C.

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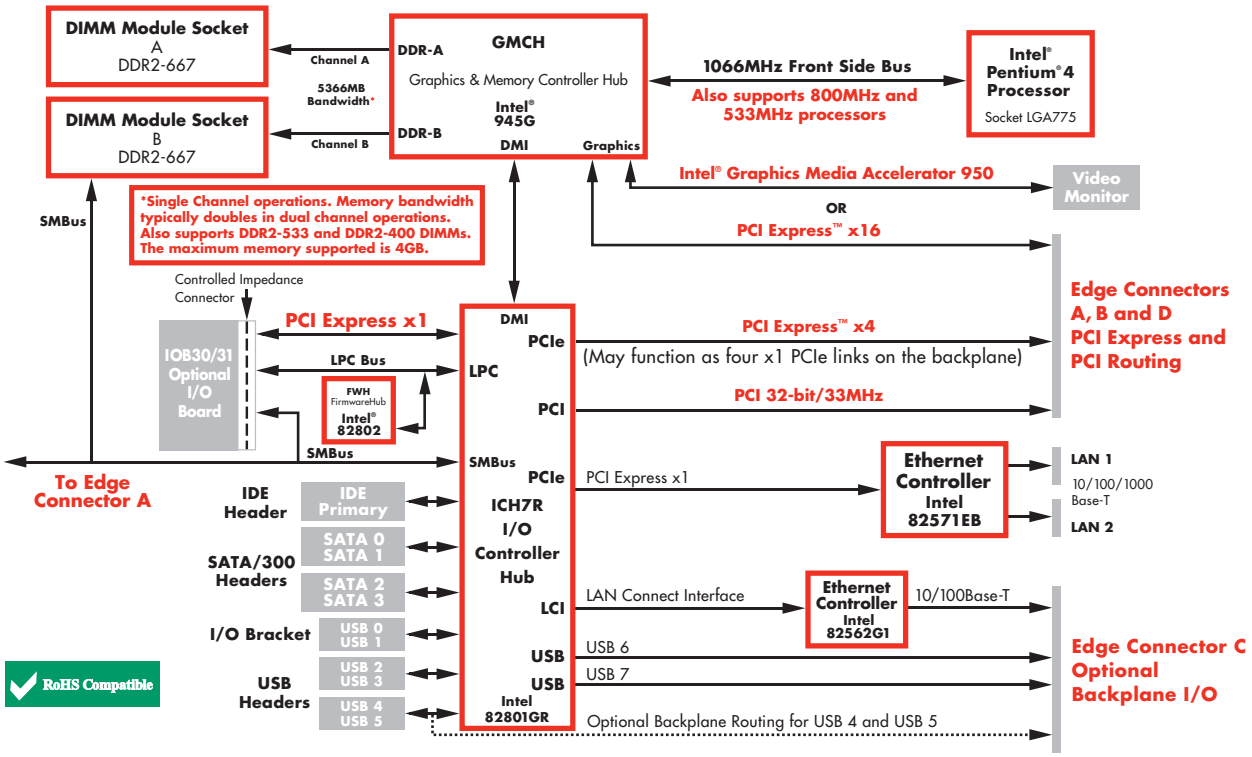

EIGHT UNIVERSAL SERIAL BUS INTERFACES (USB 2.0):

A total of eight USB 2.0 interfaces are supported by the T4L. USB ports 0 and 1 are on the I/O bracket and ports 2, 3, 4 and 5 have header connectors on the T4L. USB ports 4 and 5 can be routed to edge connector C for use on a PICMG® 1.3 backplane. The backplane routing for USB 4 and 5 is a factory-build option. Contact Trenton for ordering details. USB ports 6 and 7 are routed directly to the T4L's edge connector C.

BIOS (FLASH):

The T4L uses AMIBIOS8®. The flash BIOS resides in the SHB's Firmware Hub (FWH). AMIBIOS8 contains features such as:

- Support for flash devices for BIOS upgrading
- Integrated support for USB mass storage devices such as USB, CD-ROM, CD-RW, etc.
- Boot from network, USB mass storage devices, IDE or ATAPI
- Serial port console redirection to support headless operation (requires optional IOB30/IOB31)
- SATA/ATA/ATAPI support includes 48-bit LBA addressing to support SATA/ATA/IDE hard drive capacities over 137GB

AGENCY APPROVALS:

Designed for UL60950, CAN/CSA C22.2 No. 60950-00, EN55022:1998 Class B, EN61000-4-2:1995, EN61000-4-3:1997, EN61000-4-4:1995, EN61000-4-5:1995, EN61000-4-6:1996, EN61000-4-11:1994

STANDARDS:

- PCI Express™ Base Specification 1.0a
- SHB Express™ System Host Board PCI Express Specification - PCI Industrial Computer Manufacturers Group (PICMG®) 1.3

T4L APPLICATION CONSIDERATIONS:

Power Requirements:

Typical Values - CPU Idle State:

CPU Speed	Intel® No.	+5V	+12V	+3.3V
3.4GHz	651	2.56A	1.53A	3.27A
3.0GHz	531	2.40A	2.50A	3.27A

Typical Values - 100% CPU Stress State:

CPU Speed	Intel® No.	+5V	+12V	+3.3V
3.4GHz	651	3.60A	4.42A	3.27A
3.0GHz	531	2.64A	6.70A	3.27A

-12V @ <100mA

Tolerance for all voltages is +/- 5% and must be applied by the PICMG 1.3 backplane to edge connector C.

All processors listed are Intel® Pentium® 4

Temperature/Environment:

Operating Temperature: 0° to 45° C.
Storage Temperature: - 40° to 70° C.
Humidity: 5% to 90% non-condensing

Mechanical:

In a typical backplane, the T4L's cooling solution enables placement of option cards approximately 2.38" (60.45mm) away from the top component side of the SHB. The T4L's overall dimensions are 13.330" (33.858cm) L x 4.976" (12.639cm) H. The relative PICMG 1.3 SHB height off the backplane is the same as a PICMG 1.0 SBC due to the shorter PCI Express backplane connectors.

ADDITIONAL T4L FEATURES:

System Hardware Monitor:

The functions monitored are:

- Voltage: +3.3V, +/-12V, +5V and VCORE
- Fan speed
- Temperature

ADDITIONAL T4L FEATURES:

I/O Features:

One EIDE Ultra ATA/100 interface
Optional IOB30 I/O plug-in expansion board includes:

- Enhanced bi-directional parallel interface
- PS/2 mouse and keyboard interface (mini DIN connector)
- Floppy drive interface
- Two high-speed serial ports

Watchdog Timer:

The programmable watchdog timer is supported directly by the I/O Controller Hub. Two operating modes, free-running and one-shot, are available with this two-stage watchdog timer. Stage one can generate IRQ, SMI or SCI. Stage two generates a programmable watchdog timer reset with a total range of 1ms to 10 minutes.

ORDERING INFORMATION:

Model Name: T4L

Model #	CPU Speed	Intel® No.	Embedded CPU
6483-104-xM	3.4GHz	651	Yes
6483-052-xM	3.0GHz	531	Yes

(xM = Memory)

The stated bus speed, memory and communication interface speeds are component maximums; actual system performance may vary.

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